SONY

CXA3266Q

PLL IC for LCD Monitor/Projector

Preliminary

Description

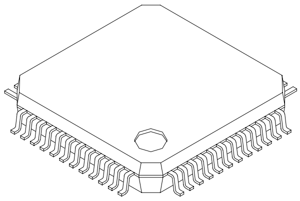
The CXA3266Q is a PLL IC for LCD monitors/projectors with built-in phase detector, charge pump, VCO and counter.

The various internal settings are performed by serial data via a 3-line bus.

Applicable LCD monitor/projector resolution are NTSC, PAL, VGA, SVGA, XGA, SXGA and UXGA etc.

The CXA3266Q is the same package as the previous CXA3106Q and CXA3106AQ. They have the same pin configuration excluding Pin 38.

48 pin QFP (Plastic)



Features

- Supply voltage: 5 ± 0.25V single power supply
- Package: 48-pin QFP
- Power consumption: 328mW
- Sync input frequency: 10 to 120kHz
- Clock output signal frequency: 10 to 203MHz
- Clock delay: 1/32 to 40/32 CLK
- Sync delay: 1/32 to 40/32 CLK
- I/O level: TTL, PECL (complementary)
- Low clock jitter
- 1/2 clock output
- TTL output high level control function

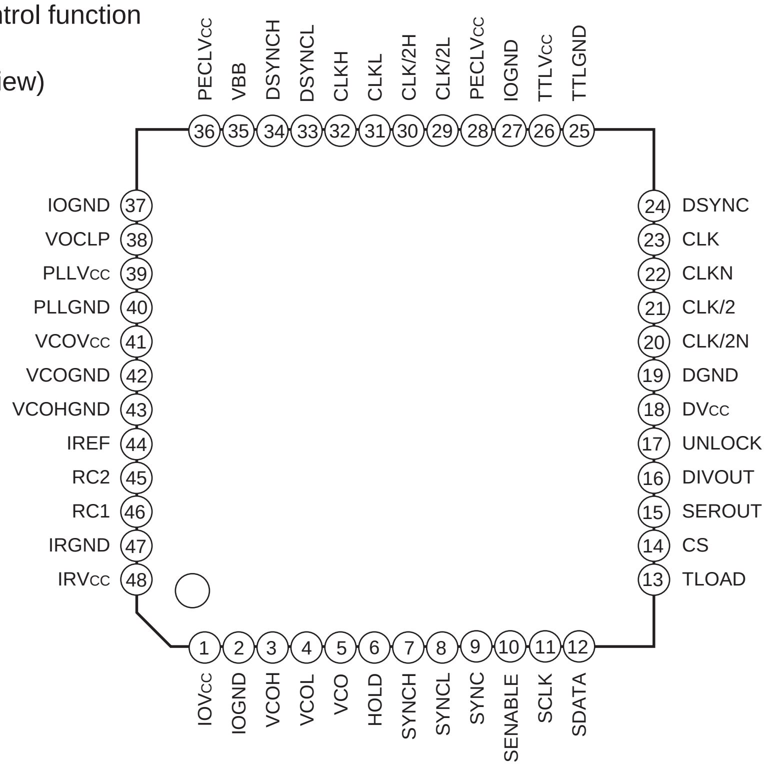
Functions

- Phase detector enable
- UNLOCK output
- Output TTL disable function
- Power saving function (2 steps)

Applications

- CRT displays
- LCD projectors
- LCD monitors
- Multi-media
- Digital TV

Pin Configuration (Top View)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	IOVcc, DVcc, TTLVcc, PECLVcc, PLLVcc, VCOVcc, IRVcc,	–0.5 to +7.0	V
	IOGND, DGND, TTLGND, VCOHGND, PLLGND, VCOGND, IRGND	–0.5 to +0.5	V
• Input voltage	VCOH, VCOL, SYNCH, SYNCL, VCO, HOLD, SYNC, SENABLE, SCLK, SDATA, TLOAD, CS, VOCLP	IOGND – 0.5 to IOVcc + 0.5	V
	RC2	IRGND – 0.5 to IRVcc + 0.5	V
• Output current	SEROUT, DIVOUT, UNLOCK, CLK/2N, CLK/2, CLKN, CLK, DSYNC, CLK/2L, CLK/2H, CLKL, CLKH, DSYNCH, DSYNCL, VBB	–30 to +30	mA
	IREF, RC1	–2 to +2	mA
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	860	mW

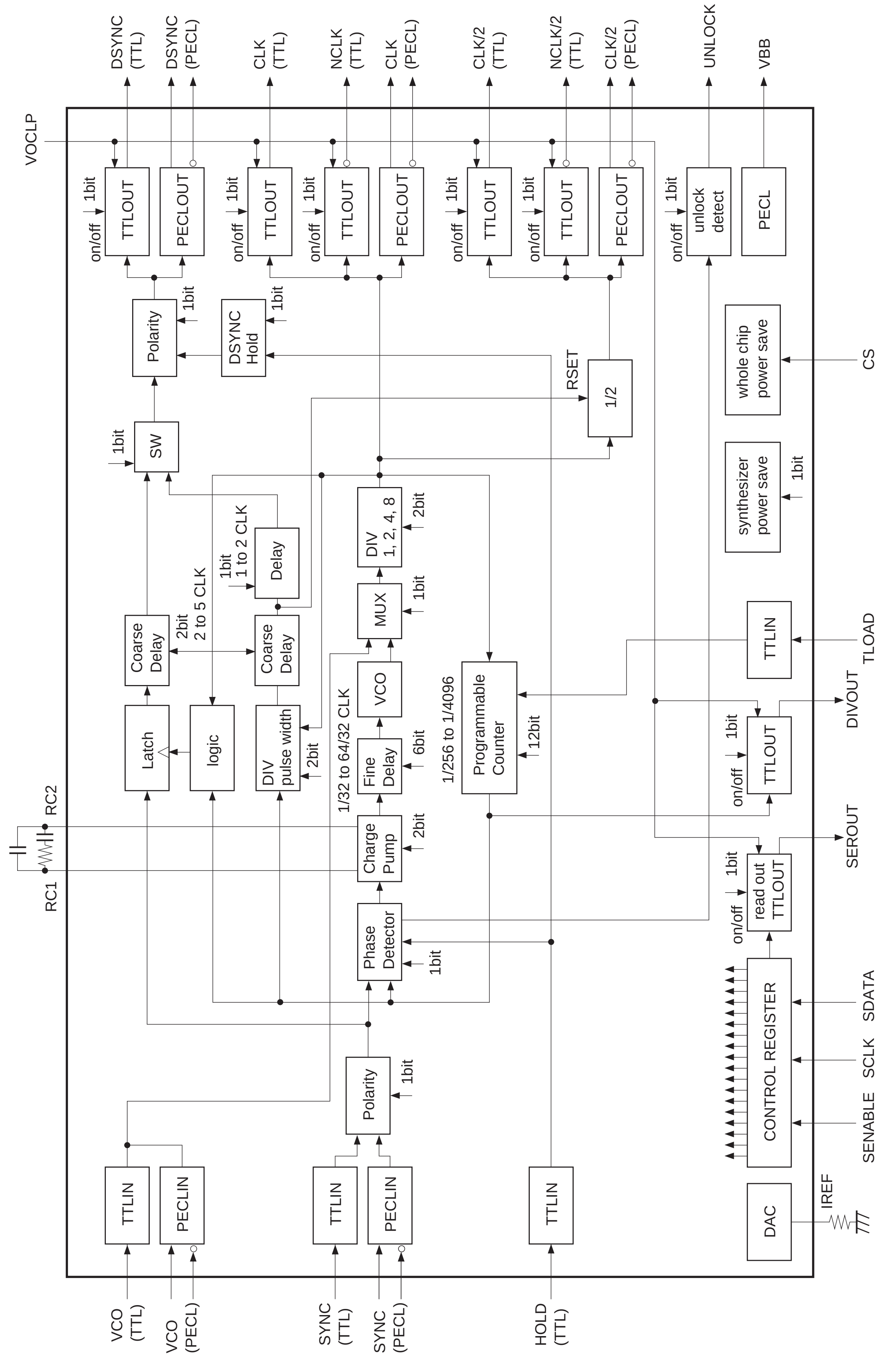
Recommended Operating Conditions

		Min.	Typ.	Max.	
• Supply voltage	IOVcc, DVcc, TTLVcc, PECLVcc, PLLVcc, VCOVcc, IRVcc	4.75	5.00	5.25	V
	IOGND, DGND, TTLGND, VCOHGND, PLLGND, VCOGND, IRGND	–0.05	0	0.05	V
• Digital input	DIN (PECL) *1 H level	IOVcc – 1.1			
	DIN (PECL) *1 L level			IOVcc – 1.5	V
	DIN (TTL) *2 H level	2.0			V
	DIN (TTL) *2 L level			0.8	V
	VOCLP (clamp voltage)	TTLGND + 2.4		TTLVcc	V
• SYNC, SYNCH, SYNCL input jitter					ns
• Operating ambient temperature	Ta	–20		+75	°C

*1 VCOH, VCOL, SYNCH, SYNCL

*2 VCO, HOLD, SYNC, SENABLE, SCLK, SDATA, TLOAD, CS

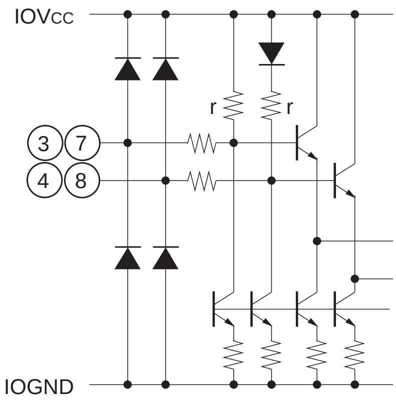
Block Diagram

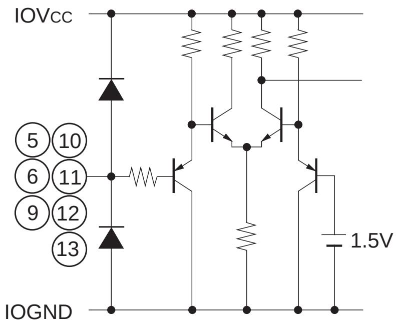


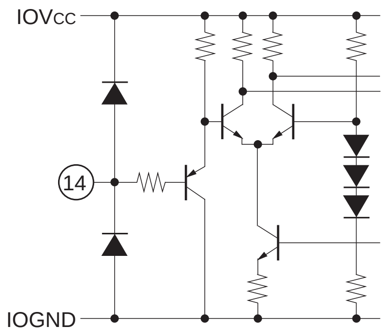
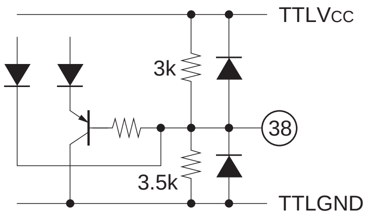
Pin No.	Symbol	Description	Reference voltage level
1	IOVcc	Digital power supply	5V
2	IOGND	Digital GND	0V
3	VCOH	External VCO input	PECL
4	VCOL	External inverted VCO input	PECL
5	VCO	External VCO input	TTL
6	HOLD	Phase detector disable signal input	TTL
7	SYNCH	Sync input	PECL
8	SYNCL	Inverted sync input	PECL
9	SYNC	Sync input	TTL
10	SENABLE	Control signal (enable)	TTL
11	SCLK	Control signal (clock)	TTL
12	SDATA	Control signal (data)	TTL
13	TLOAD	Programmable counter test input	TTL
14	CS	Chip select	TTL
15	SEROUT	Register read output	TTL
16	DIVOUT	Programmable counter test output	TTL
17	UNLOCK	Unlock signal output	TTL
18	DVcc	Digital power supply	5V
19	DGND	Digital GND	0V
20	CLK/2N	Inverted 1/2 clock output	TTL
21	CLK/2	1/2 clock output	TTL
22	CLKN	Inverted clock output	TTL
23	CLK	Clock output	TTL
24	DSYNC	Delay sync signal output	TTL
25	TTLGND	TTL output GND	0V
26	TTLVcc	TTL output power supply	5V
27	IOGND	Digital GND	0V
28	PECLVcc	PECL output power supply	5V
29	CLK/2L	Inverted 1/2 clock output	PECL
30	CLK/2H	1/2 clock output	PECL
31	CLKL	Inverted clock output	PECL
32	CLKH	Clock output	PECL
33	DSYNCL	Delay sync signal output	PECL
34	DSYNCH	Inverted delay sync signal output	PECL
35	VBB	PECL reference voltage	PECLVcc – 1.7V
36	PECLVcc	PECL output power supply	5V
37	IOGND	Digital GND	0V
38	VOCLP	TTL high level clamp	Clamp voltage
39	PLLVcc	PLL circuit analog power supply	5V
40	PLLGND	PLL circuit analog GND	0V
41	VCOVcc	VCO circuit analog power supply	5V
42	VCOGND	VCO circuit analog GND	0V
43	VCOHGND	VCO SUB analog GND	0V
44	IREF	Charge pump current preparation	1.2V
45	RC2	External pin for LPF	2.0 to 4.4V
46	RC1	External pin for LPF	2.1V
47	IRGND	IREF analog GND	0V
48	IRVcc	IREF analog power supply	5V

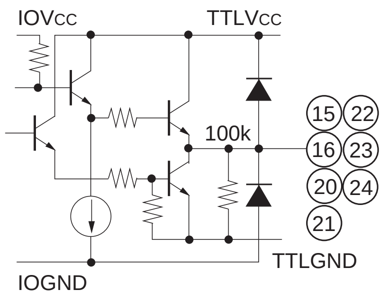
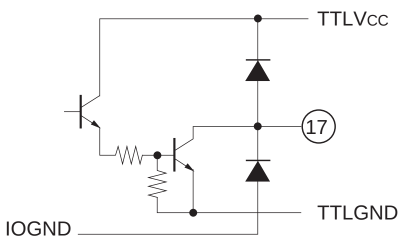
Pin Description and I/O Pin Equivalent Circuit

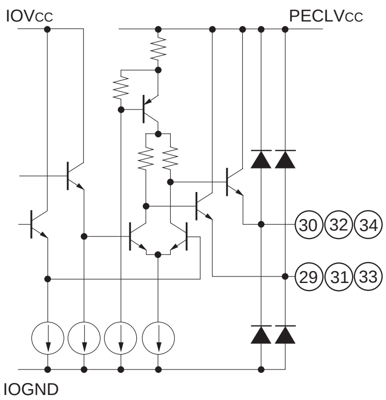
Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
1	IOVcc	—	5V		Digital power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
2	IOGND	—	0V		Digital GND.
18	DVcc	—	5V		Digital power supply.
19	DGND	—	0V		Digital GND.
25	TTLGND	—	0V		TTL output GND.
26	TTLVcc	—	5V		TTL output power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
27	IOGND	—	0V		Digital GND.
28	PECLVcc	—	5V		PECL output power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
36	PECLVcc	—	5V		PECL output power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
37	IOGND	—	0V		Digital GND.
39	PLLVcc	—	5V		PLL circuit analog power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
40	PLLGND	—	0V		PLL circuit analog GND.
41	VCOVcc	—	5V		VCO circuit analog power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
42	VCOGND	—	0V		VCO circuit analog GND.
43	VCOHGND	—	0V		VCO SUB analog GND.
47	IRGND	—	0V		IREF analog GND.
48	IRVcc	—	5V		IREF analog power supply. Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.

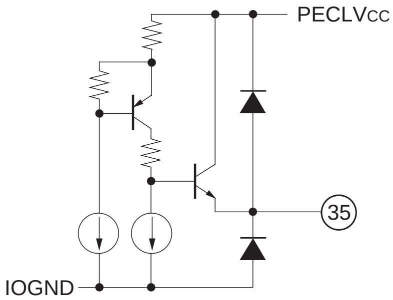
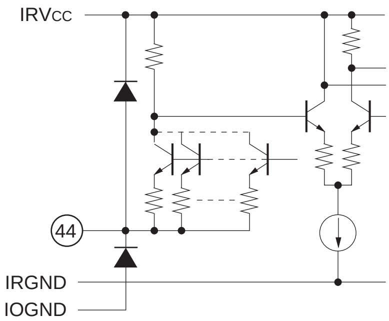
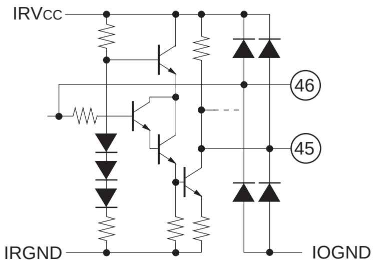
Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
3	VCOH	I	PECL		External VCO input. Programmable counter test input (switchable by a control register). When using the VCO PECL input, open the Pin 5 VCO TTL input.
4	VCOL	I	PECL		External inverted VCO input. When open, this pin goes to the PECL threshold voltage (IOVcc – 1.3V). Only the Pin 3 VCOH input with VCOL input open can be also operated but complementary input is recommended in order to realize stable high-speed operation.
7	SYNCH	I	PECL		Sync input. When using the SYNCH PECL input, open the Pin 9 SYNC TTL input. The sync signal can be switched between positive/negative polarity by an internal register.
8	SYNCL	I	PECL		Inverted sync input. When open, this pin goes to the PECL threshold voltage (IOVcc – 1.3V). Only the Pin 7 SYNCH input with SYNCL input open can be also operated but complementary input is recommended in order to realize stable high-speed operation.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
5	VCO	I	TTL		External VCO input. Programmable counter test input (controlled by a control register). When using the VCO TTL input, open the Pin 3 VCOH and Pin 4 VCOL PECL inputs.
6	HOLD	I	TTL		Phase detector disable signal. Active high. When this pin is high, the phase detector output is held. This pin goes to high level when open. (See the HOLD Timing Chart.)
9	SYNC	I	TTL		Sync input. When using the SYNC TTL input, open the Pin 7 SYNCH and Pin 8 SYNCL PECL inputs. The sync signal can be switched between positive/negative polarity by an internal register.
10	SENABLE	I	TTL		Control signal (enable) for setting the internal registers. When SENABLE is low, registers can be written; when high, registers can be read. (See the Control Register Table and Control Timing Chart.)
11	SCLK	I	TTL		Control signal (clock) for setting the internal registers. When SENABLE is low, SDATA is loaded to the registers at the rising edge of SCLK. When SENABLE is high, the register contents are output from SEROUT at the falling edge of SCLK. (See the Control Register Table and Control Timing Chart.)
12	SDATA	I	TTL		Control signal (data) for setting the internal registers. (See the Control Register Table and Control Timing Chart.)
13	TLOAD	I	TTL		Programmable counter test input. This pin is normally open status and high. Register contents can be loaded immediately to programmable counter by setting TLOAD low during the programmable counter test mode.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
14	CS	I	TTL		Chip select. When low, all circuits including the register circuit are set to the power saving mode. When high, all circuits are set to operating mode.
38	VOCLP	I	Clamp voltage		TTL output high level clamp. The TTL high level voltage is clamped at the almost same value with the voltage applied to this pin. When this pin is open, TTL output high level is approximately 2.7V.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
15	SEROUT	O	TTL		Register read output. When SENABLE is high, the register contents are output from SEROUT at the falling edge of SCLK. (See the Control Register Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
16	DIVOUT	O	TTL		Programmable counter test output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
20	CLK/2N	O	TTL		Inverted 1/2 clock output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
21	CLK/2	O	TTL		1/2 clock output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
22	CLKN	O	TTL		Inverted clock output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
23	CLK	O	TTL		Clock output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.
24	DSYNC	O	TTL		Delay sync signal output. (See the I/O Timing Chart.) TTL output can be turned ON/OFF (high impedance) and switched between positive/negative polarity by a control register.
17	UNLOCK	O	TTL		Unlock signal output. This pin is an open collector output, and pulls in the current when a phase difference occurs. The UNLOCK sensitivity can be adjusted by connecting a capacitor and resistors to this output appropriately. (See the UNLOCK Timing Chart.) TTL output can be turned ON/OFF (high impedance) by a control register.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
29	CLK/2L	O	PECL		Inverted 1/2 clock output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.
30	CLK/2H	O	PECL		1/2 clock output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.
31	CLKL	O	PECL		Inverted clock output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.
32	CLKH	O	PECL		Clock output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.
33	DSYNCL	O	PECL		Delay sync signal output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.
34	DSYNCH	O	PECL		Inverted delay sync signal output. (See the I/O Timing Chart.) This pin requires an external pull-down resistor. When not used, connect to PECLVcc without connecting a pull-down resistor.

Pin No.	Symbol	I/O	Reference voltage level	Equivalent circuit	Description
35	VBB	O	PECLVcc –1.7V		PECL reference voltage. When used, ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
44	IREF	—	1.2V		Charge pump current preparation. Connect to GND via an external resistor (3.0kΩ). Ground this pin to the ground pattern with a 0.1µF ceramic chip capacitor as close to the pin as possible.
45	RC2	—	2.0 to 4.4V		External pin for LPF. See the Recommended Operating Circuit for the external circuits. Note that external resistors and capacitors should be metal film resistors and temperature compensation capacitors which are relatively unaffected by temperature change.
46	RC1	—	2.1V		External pin for LPF. See the Recommended Operating Circuit for the external circuits.

Control Register Table

		DATA								ADDRESS		
Register No.	Register Name	DATA7 MSB	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0 LSB	ADDR2 MSB	ADDR1	ADDR0 LSB
Register 1	register read no	1	2	3	4	5	6	7	8			
	DIVREG1	VCO DIV Bit 7	VCO DIV Bit 6	VCO DIV Bit 5	VCO DIV Bit 4	VCO DIV Bit 3	VCO DIV Bit 2	VCO DIV Bit 1	VCO DIV Bit 0	0	0	1
Register 2	register read no					9	10	11	12			
	DIVREG2					VCO DIV Bit 11	VCO DIV Bit 10	VCO DIV Bit 9	VCO DIV Bit 8	0	1	0
Register 3	register read no							13	14			
	CENFREREG							DIV 1, 2, 4, 8 Bit 1	DIV 1, 2, 4, 8 Bit 0	0	1	1
Register 4	register read no	15	16	17	18	19	20	21	22			
	DELAYREG	COARSE DELAY Bit 1	COARSE DELAY Bit 0	FINE DELAY Bit 5	FINE DELAY Bit 4	FINE DELAY Bit 3	FINE DELAY Bit 2	FINE DELAY Bit 1	FINE DELAY Bit 0	1	0	0
Register 5	register read no			23	24	25	26	27	28			
	CPREG			DSYNC DELAY	DSYNC WIDTH Bit 1	DSYNC WIDTH Bit 0	PD POL	C.Pump Bit 1	C.Pump Bit 0	1	0	1
Register 6	register read no	29	30	31	32	33	34	35	36			
	TTLPOLREG	UNLOCK Enable	DSYNC Enable	NCLK/2 Enable	CLK/2 Enable	NCLK Enable	CLK Enable	DSYNC POL	SYNC POL	1	1	0
Register 7	register read no			37	38	39	40	41	42			
	TESTPOWREG			DSYNC Hold	DSYNC By-pass	DIVOUT Enable	Read out power	Synth power	VCO By-pass	1	1	1

Electrical Characteristics (Ta = 25°C, V_{CC} = 5V, GND = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption (excluding output current)						
Current consumption 1	$I_{CC}1$	CS = H, Synth Power = 1		65.5		mA
Current consumption 2	$I_{CC}2$	CS = H, Synth Power = 0		13.0		mA
Current consumption 3	$I_{CC}3$	CS = L		1.5		mA
Digital input						
Digital high level input voltage (PECL)	$V_{IH}1$		IOV_{CC} –1.15			V
Digital low level input voltage (PECL)	$V_{IL}1$				IOV_{CC} –1.5	V
VCOL, SYNCL input open voltage (PECL)	V_{IO}			IOV_{CC} –1.3		V
Digital high level input current (PECL)	$I_{IH}1$	V_{IH} = IOV_{CC} – 0.8V	–100		100	µA
Digital low level input current (PECL)	$I_{IL}1$	V_{IL} = IOV_{CC} – 1.6V	–200		0	µA
Digital high level input voltage (TTL)	$V_{IH}2$		2.0			V
Digital low level input voltage (TTL)	$V_{IL}2$				0.8	V
Digital high level input current (TTL)	$I_{IH}2$	V_{IH} = 3.5V	–10		–5	µA
Digital low level input current (TTL)	$I_{IL}2$	V_{IL} = 0.2V	–20		0	µA
HOLD characteristics						
RC1 input pin leak current	Ileak				1.00	nA
HOLD signal set-up time	Ths		20			ns
HOLD signal hold time	Thh		20			ns
Digital output						
Digital high level output voltage (PECL)	$V_{OH}1$	RL = 330Ω	$PECLV_{CC}$ –1.6			V
Digital low level output voltage (PECL)	$V_{OL}1$	RL = 330Ω			$PECLV_{CC}$ –1.8	V
PECL output reference voltage	VBB	RL = 330Ω		$PECLV_{CC}$ –1.7		V
Digital high level output voltage (TTL)	$V_{OH}2$	CL = 10pF	2.4			V
Digital low level output voltage (TTL)	$V_{OL}2$	CL = 10pF			0.5	V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
UNLOCK output						
UNLOCK output current	Iunlock		–30			mA
SYNC input						
SYNC input frequency range	Fin		10		120	kHz
DSYNC output						
DSYNC output coarse delay time setting resolution (upper)	Rdsync1			2		bit
DSYNC output coarse delay time (upper)	Td1		2		5	CLK
DSYNC output fine delay time setting resolution (lower)	Rdsync2			6		bit
DSYNC output fine delay time (lower)	Td2		1/32		40/32	CLK
DSYNC output DIVOUT output delay time	Td9		4		5	CLK
VCO characteristics						
DIV output frequency operation range 1	Fvco1	DIV = 1/1	40		203	MHz
DIV output frequency operation range 2	Fvco2	DIV = 1/2	20		100	MHz
DIV output frequency operation range 3	Fvco3	DIV = 1/4	10		50	MHz
DIV output frequency operation range 4	Fvco4	DIV = 1/8	5		25	MHz
VCO lock range	Vlock		2.0		4.4	V
VCO gain 1	Kvco1	DIV = 1/1		480		Mrad/sv
VCO gain 2	Kvco2	DIV = 1/2		240		Mrad/sv
VCO gain 3	Kvco3	DIV = 1/4		120		Mrad/sv
VCO gain 4	Kvco4	DIV = 1/8		60		Mrad/sv
Charge pump current 1	Kpd1	C.Pump Bit = 00, IREF = 3.0kΩ		100		µA
Charge pump current 2	Kpd2	C.Pump Bit = 01, IREF = 3.0kΩ		200		µA
Charge pump current 3	Kpd3	C.Pump Bit = 10, IREF = 3.0kΩ		400		µA
Change pump current 4	Kpd4	C.Pump Bit = 11, IREF = 3.0kΩ		800		µA
VCO counter bits	Rdiv2			12		bit

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK (CLK, CLK/2) output						
CLK output (PECL) frequency range 1	Fclk1PECL	DIV = 1/1	40		203	MHz
CLK output (PECL) frequency range 2	Fclk2PECL	DIV = 1/2	20		100	MHz
CLK output (PECL) frequency range 3	Fclk3PECL	DIV = 1/4	10		50	MHz
CLK output (PECL) frequency range 4	Fclk4PECL	DIV = 1/8	5		25	MHz
CLK, CLK/2 output (PECL) rise time	TrPECL	10% to 90%, RL = 330Ω	1.0	1.5	2.0	ns
CLK, CLK/2 output (PECL) fall time	TfPECL	10% to 90%, RL = 330Ω	1.0	1.5	2.0	ns
CLK output (TTL) frequency range 1	Fclk1TTL	DIV = 1/1	40		100	MHz
CLK output (TTL) frequency range 2	Fclk2TTL	DIV = 1/2	20		100	MHz
CLK output (TTL) frequency range 3	Fclk3TTL	DIV = 1/4	10		50	MHz
CLK output (TTL) frequency range 4	Fclk4TTL	DIV = 1/8	5		25	MHz
CLK, CLK/2 output (TTL) rise time	TrTTL	10% to 90%, CL = 10pF		1.1		ns
CLK, CLK/2 output (TTL) fall time	TfTTL	10% to 90%, CL = 10pF		1.1		ns
CLK output (PECL, TTL) duty	Dclk2	CL = 10pF	40	50	60	%
SYNC input (PECL) and CLK output (PECL) delay offset	Td3	CL = 10pF	1.0	1.6	2.2	ns
CLK output (PECL) and DSYNC output (PECL) phase difference	Td4	CL = 10pF	1.0	2.0	3.0	ns
CLK output (PECL) and CLK/2 output (PECL) phase difference	Td5	CL = 10pF	0.3	0.7	1.1	ns
DSYNC, CLK, CLK/2 output (PECL) and TTL output phase difference	Td8	CL = 10pF	1.8	2.5	3.2	ns

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CLK (CLK, CLK/2) output						
CLK vs. SYNC output jitter (NTSC)	Tj1p-p	triggered at SYNC Fsync = 15.73kHz Fclk = 12.27MHz N = 780		2.1		ns
CLK vs. SYNC output jitter (VGA)	Tj2p-p	triggered at SYNC Fsync = 31.47kHz Fclk = 25.18MHz N = 800		1.5		ns
CLK vs. SYNC output jitter (SVGA)	Tj3p-p	triggered at SYNC Fsync = 48.08kHz Fclk = 50.00MHz N = 1040		1.4		ns
CLK vs. SYNC output jitter (XGA)	Tj4p-p	triggered at SYNC Fsync = 56.48kHz Fclk = 75.00MHz N = 1328		1.4		ns
CLK vs. SYNC output jitter (SXGA)	Tj5p-p	triggered at SYNC Fsync = 80kHz Fclk = 136.00MHz N = 1700		1.0		ns
CLK vs. SYNC output jitter (UXGA)	Tj6p-p	triggered at SYNC Fsync = 93.75kHz Fclk = 202.50MHz N = 2160		0.8		ns
CLK vs. DSYNC output jitter	Tj7p-p	triggered at DSYNC			0.1	ns
Control registers						
SCLK frequency	SCLK	in write/read mode			12	MHz
SENABLE set-up time	TENS	in write mode	3			ns
SENABLE hold time	TENH	in write mode	0			ns
SDATA set-up time	TDS	in write mode	3			ns
SDATA hold time	TDH	in read mode	0			ns
SENABLE set-up time	TNENS	in read mode	3			ns
SENABLE hold time	TNENH	in read mode	0			ns

Description of Block Diagram

Sync Input

Sync signals in the range of 10 to 120kHz can be input. Input supports both positive and negative polarity. PECL input can also be a single input.
When SYNC is positive polarity, the clock is regenerated in synchronization with the rising edge of the sync signal.
When SYNC is negative polarity, the clock is regenerated in synchronization with the falling edge of the sync signal.
VCO oscillation stops when there is no sync input.

Register: SYNC POL	1	0
SYNC input polarity	Positive	Negative

Phase Detector

The phase detector operates at the sync input frequency of 10 to 120kHz. The PD input polarity should be set to the default PD POL = 1. Phase comparison is performed at the edges.
The input circuit of the phase detector does not contain a hysteresis circuit, so the waveform must be shaped at the front end of the CXA3266Q when inputting a noisy signal.

The phase detector HOLD signal is supplied by TTL. (See the HOLD Timing Chart.)

The PLL UNLOCK signal is output by an open collector.
(See the UNLOCK Timing Chart.)

Charge Pump

The gain (I, I/2, I/4, I/8) can be varied by changing the charge pump current using 2 bits of control register.

Register: C.Pump bit 1	0	0	1	1
Register: C.Pump bit 0	0	1	0	1
Charge pump current	100µA	200µA	400µA	800µA

LPF

This is a loop filter comprised of the external capacitors and resistor.
Be sure to use metal film resistors with little temperature variation and a temperature-compensated capacitor.
In particular, the 0.068µF capacitor should be equivalent to high dielectric constant series capacitor type B or better. (electrostatic capacitance change ratio ±10%: T = –25 to +85°C)

VCO

The VCO oscillator frequency covers from 40 to 203MHz.

VCO Rear-end Counter

The VCO output is frequency divided to 1/1, 1/2, 1/4 or 1/8 by switching 2 bits of control register.
The operating range can be expanded to 5 to 203MHz by combining the counter with a VCO frequency divider.

Register: DIV 1, 2, 4, 8 bit 1	0	0	1	1
Register: DIV 1, 2, 4, 8 bit 0	0	1	0	1
Counter frequency divisions	1/1	1/2	1/4	1/8

Feedback Programmable Counter

This counter can be set as desired from 256 to 4096 using 12 bits.

Frequency divisions = (m + 1) × 8 + n, n: 3 bits (VCO DIV bits 0 to 2), m: 9 bits (VCO DIV bits 3 to 11)

When the register value is changed, the new setting is actually loaded to the counter when the counter value becomes "all 0".

Clock Output

When SYNC input is positive polarity, the clock is regenerated in synchronization with the rising edge of the sync signal.

The clock output delay time can be changed in the range of 1/32 to 40/32 CLK using 6 bits of control register. (See the I/O Timing Chart.)

Output is TTL and PECL (complementary), and supports both positive and negative polarity. Clock TTL output can also be turned off independently.

Register: Clock Enable	1	0
Clock output status	ON	OFF

1/2 Clock Output

Reset is performed at the delay sync timing and the clock output is frequency divided by 1/2. (See the I/O Timing Chart.)

Both odd and even output are TTL and PECL output. TTL output can also be turned off independently.

Register: Clock Enable	1	0
Clock output status	ON	OFF

Delay Sync Output

The front edge of the delay sync pulse is latched by the pulse obtained by frequency dividing the CLK regenerated by the PLL, so there is almost no jitter with respect to CLK. This front edge can be used as the reset signal for the system timing circuit.

The rear edge of the delay sync pulse is latched by the CLK regenerated by the PLL. This relationship is undefined for one clock as shown in the Timing Chart.

The delay sync output delay time can be varied in two stages. First, the delay time can be varied in the range of 1/32 to 40/32 CLK using 6 bits of control register, and then in the range of 2 to 5 CLK using 2 bits of control register. In other words, the total delay time is ((1/32 to 40/32) + (2 to 5)) CLK. (See the I/O Timing Chart.)

DSYNC output is TTL and PECL (complementary), and supports both positive and negative polarity. Clock TTL output can also be turned off.

Register: Clock Enable	1	0
Clock output status	ON	OFF

Lower delay line FINE DELAY bits 0 to 4	000000	000001	. . . .	101000
Delay time	1/32CLK	2/32CLK	. . . .	40/32CLK

Upper delay line COARSE DELAY bits 0 to 1	00	01	10	11
Delay time	2CLK	3CLK	4CLK	5CLK

Register: DSYNC POL	1	0
DSYNC output polarity	Positive	Negative

Programmable Counter TTL Output Switching

Output (PECL, TTL) from DSYNC output is possible by switching of control register.

Register: DSYNC By-pass	0	1
Output status from DSYNC	DIVOUT output	DSYNC output

Delay Sync Output Width (DSYNC By-pass = 0)

Delay sync output pulse width can be varied to 1, 2, 4, or 8CLK by switching 2 bits of control register.

Register: DSYNC WIDTH	00	01	10	11
DSYNC width	1CLK	2CLK	4CLK	8CLK

Delay Sync Output Delay (DSYNC By-pass = 0)

DIVOUT output delay from delay sync output can be varied to 4 or 5CLK by switching of control register.

Register: DSYNC DELAY	0	1
Delay time	4CLK	5CLK

DSYNC Output Switching during HOLD

By switching with a control register, DSYNC output during HOLD period is controlled. Its output status is different according to DSYNC By-pass, DSYNC POL and HOLD signals of the register. The output for each setting is shown below.

Register DSYNC Hold	Register DSYNC By-pass	Register DSYNC POL	Pin 6 HOLD	Output from DSYNC (Pin 24) and DSYNCH (Pin 34)
0	0	0	H	H
0	0	0	L	$\overline{\text{DIVOUT}}$
0	0	1	H	L
0	0	1	L	DIVOUT
0	1	0	H	H
0	1	0	L	$\overline{\text{DSYNC}}$
0	1	1	H	L
0	1	1	L	DSYNC
1	0	0	H	$\overline{\text{DIVOUT}}$
1	0	0	L	$\overline{\text{DIVOUT}}$
1	0	1	H	DIVOUT
1	0	1	L	DIVOUT
1	1	0	H	$\overline{\text{DSYNC}}$
1	1	0	L	$\overline{\text{DSYNC}}$
1	1	1	H	DSYNC
1	1	1	L	DSYNC

Control Circuit (3-bit address, 8-bit data)

The timing and input methods are described hereafter.

Feedback programmable counter control	REGISTER1, 2	12bit	VCODIV Bit0 to 11
VCO rear-end counter control	REGISTER3	2bit	DIV1, 2, 4, 8 Bit0, Bit1
Fine delay line control	REGISTER4	6bit	FINE DELAY Bit0 to 5
Coarse delay line control	REGISTER4	2bit	COARSE DELAY Bit0, Bit1
Charge pump current DAC control	REGISTER5	2bit	C.Pump Bit0, Bit1
Phase detector input positive/negative polarity control	REGISTER5	1bit	PD POL
Delay sync output width control	REGISTER5	2bit	DSYNC WIDTH
Delay sync output delay control	REGISTER5	1bit	DSYNC DELAY
Sync input positive/negative polarity control	REGISTER6	1bit	SYNC POL
Delay sync output positive/negative polarity control	REGISTER6	1bit	DSYNC POL
Clock TTL output OFF function	REGISTER6	1bit	CLK Enable
Inverted clock TTL output OFF function	REGISTER6	1bit	NCLK Enable
1/2 clock TTL output OFF function	REGISTER6	1bit	CLK/2 Enable
Inverted 1/2 clock TTL output OFF function	REGISTER6	1bit	NCLK/2 Enable
Delay sync TTL output OFF function	REGISTER6	1bit	DSYNC Enable
UNLOCK output OFF function	REGISTER6	1bit	UNLOCK Enable
Programmable counter input switching	REGISTER7	1bit	VCO By-pass
Power save with register contents held	REGISTER7	1bit	Synth power
Register read function power ON/OFF	REGISTER7	1bit	Read out power
Programmable counter TTL output OFF function	REGISTER7	1bit	DIVOUT Enable
Programmable counter TTL output switching	REGISTER7	1bit	DSYNC By-pass
Delay sync output hold function	REGISTER7	1bit	DSYNC Hold

Power Save

The CXA3266Q realizes 2-step power saving (all OFF, control registers only ON). This is controlled by a control register and the chip selector.

Step 1: Chip selector control

CS	H	L
Power saving status	Power ON	All OFF

Step 2: Control register control

Register: Synth power	1	0
Power saving status	Power ON	Control registers only ON

Readout Circuit (during test mode)

The control register contents can be read by serial data from SEROUT.
(See the Control Register Timing Chart.)

Register: Read out power	0	1
Readout status	Function OFF	Function ON

Programmable Counter Output (during test mode)

The programmable counter output is TTL output from the DIVOUT pin.
(See the I/O Timing Chart.)
This output is normally not used.

Register: DIVOUT Enable	0	1
DIVOUT output status	OFF	ON

TLOAD input (during test mode)

This control signal forcibly loads the control register contents to the programmable counter.
This signal is normally not used.

TLOAD	H	L
Forced load control status	Function OFF	Function ON

VCO input (during test mode)

This is the programmable counter test signal input pin.
This pin can be switched internally by the MUX circuit.
TTL and PECL input are possible.
This pin is normally not used.

Register: VCO By-pass	1	0
Input status	Internal VCO	External input

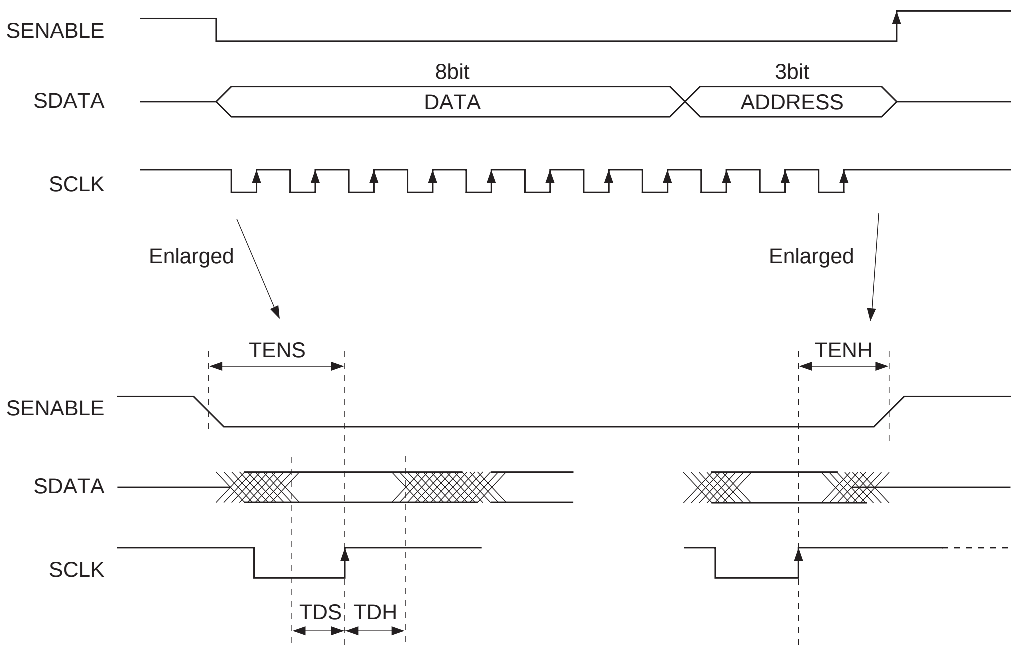
Control Register Timing

1) Write mode

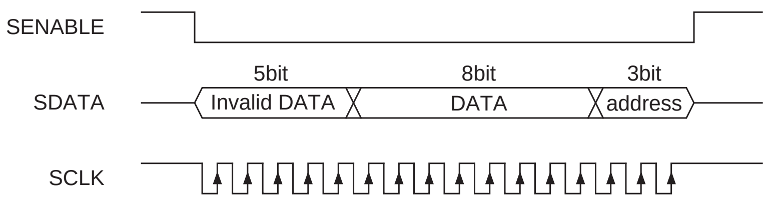
Many functions of the CXA3266Q can be controlled via a program. Characteristics are changed by setting the internal control register values via a serial interface comprised of three pins: SENABLE (Pin 10), SCLK (Pin 11) and SDATA (Pin 12). The write timing diagram is shown below.

Input the 8-bit data and 3-bit register address MSB first to the SDATA pin. Some registers are not 8 bits, but the data is input aligned with the LSB side in these cases. (See the Register Table.)

SENABLE is the enable signal and is active low. SCLK is the transfer clock signal, and data is loaded to the IC at the rising edge. When SENABLE rises, SCLK must be high. (Registers are set at the rising edge of SENABLE.) When SENABLE falls, SCLK may be either high or low.



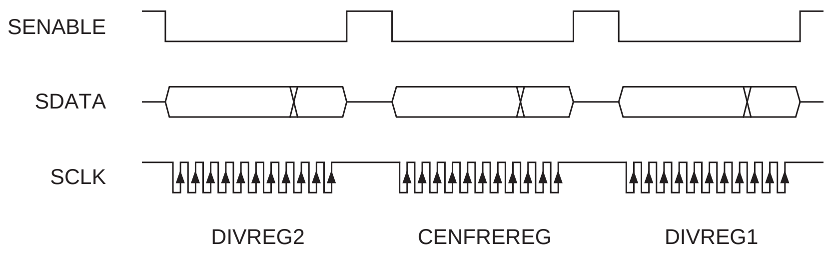
For example, when inputting a 16-bit signal, the initial 5 bits are invalid and the latter 11 bits are valid. This is to say that the latter 11 bits are loaded to the register.



The settings of the frequency divider (2 bits, DIV1, 2, 4, 8) and programmable counter (12 bits, VCODIV) at the rear end of the VCO are transferred in the order shown below. (The data will be set when the three registers are transferred.)
First DIVREG2, CENFREREG and DIVREG1 are set, and then the data is transferred independently at the timings shown below.

DIVREG2 (upper 4 bits of VCODIV)
↓
CENFREREG (2 bits of DIV1, 2, 4, 8)
↓
DIVREG1 (lower 8 bits of VCODIV)

All three of the above registers must be changed even when changing only (2 bits of DIV1, 2, 4, 8). This is the same when changing only (12 bits of VCODIV).

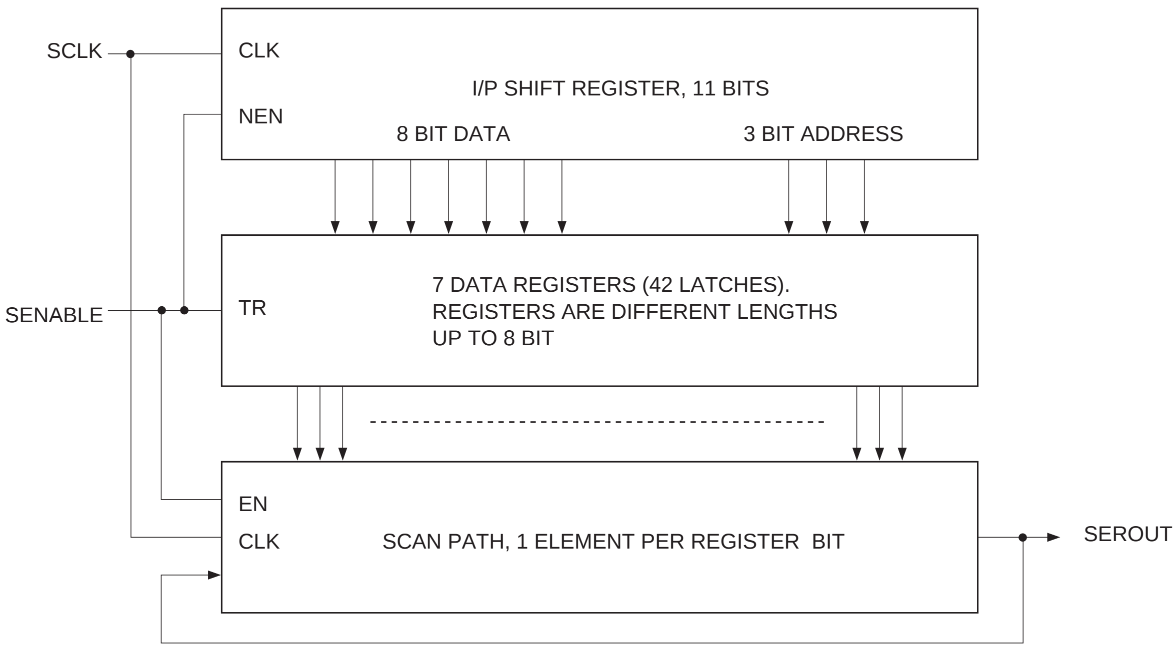


2) Read mode

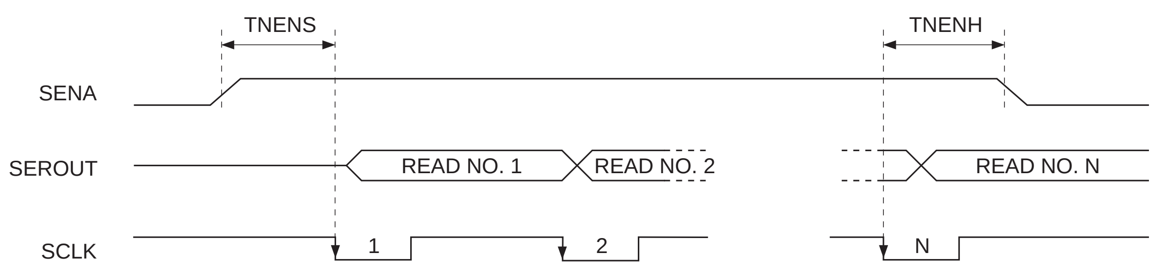
Data can be transferred from the shift register to the data register only when SENABLE is high.

Binary data can be read from the data register by inputting SCLK when SENABLE is high. Data is loaded from the data register to the SCAN PATH circuit each time one clock is input to SCLK, and is output sequentially from the register read no. 1 data (VCODIV bit 7) through the SEROUT pin. When the 42nd SCLK clock pulse is input, the register read no. 42 data (VCO By-pass) is output. Then, when the 43rd clock pulse is input to SCLK, the output returns to the register read no. 1 data (VCODIV bit 7) and the data output is repeated. Also, the data output from the SCAN PATH circuit is automatically reloaded even when the shift register data is changed during data output.

Note) Since all registers do not have 8 bits, only the valid bits of each register are loaded to the SCAN PATH circuit. (See the Control Register Table for the actual register read no.)

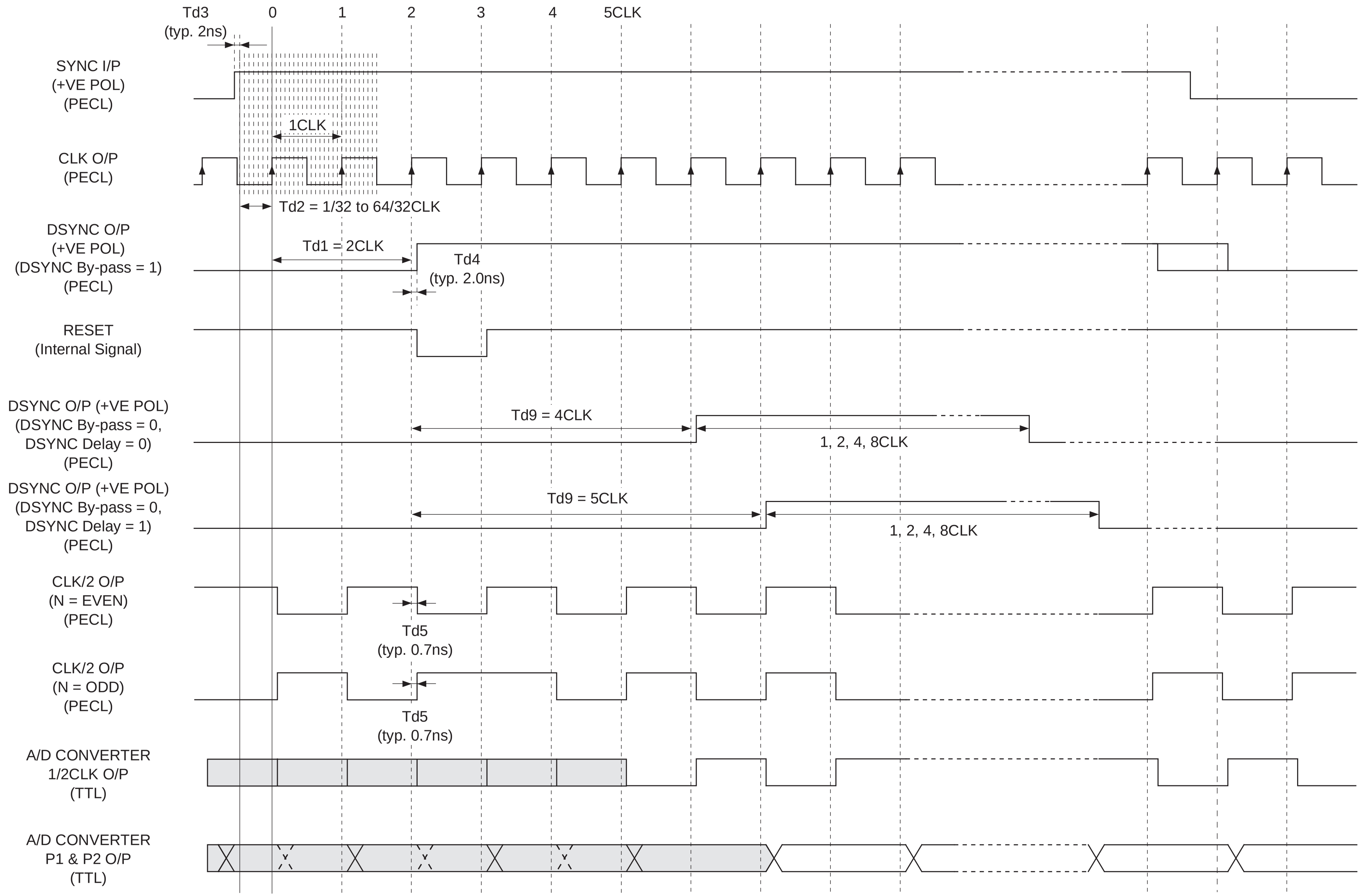


Block Diagram during Read Mode

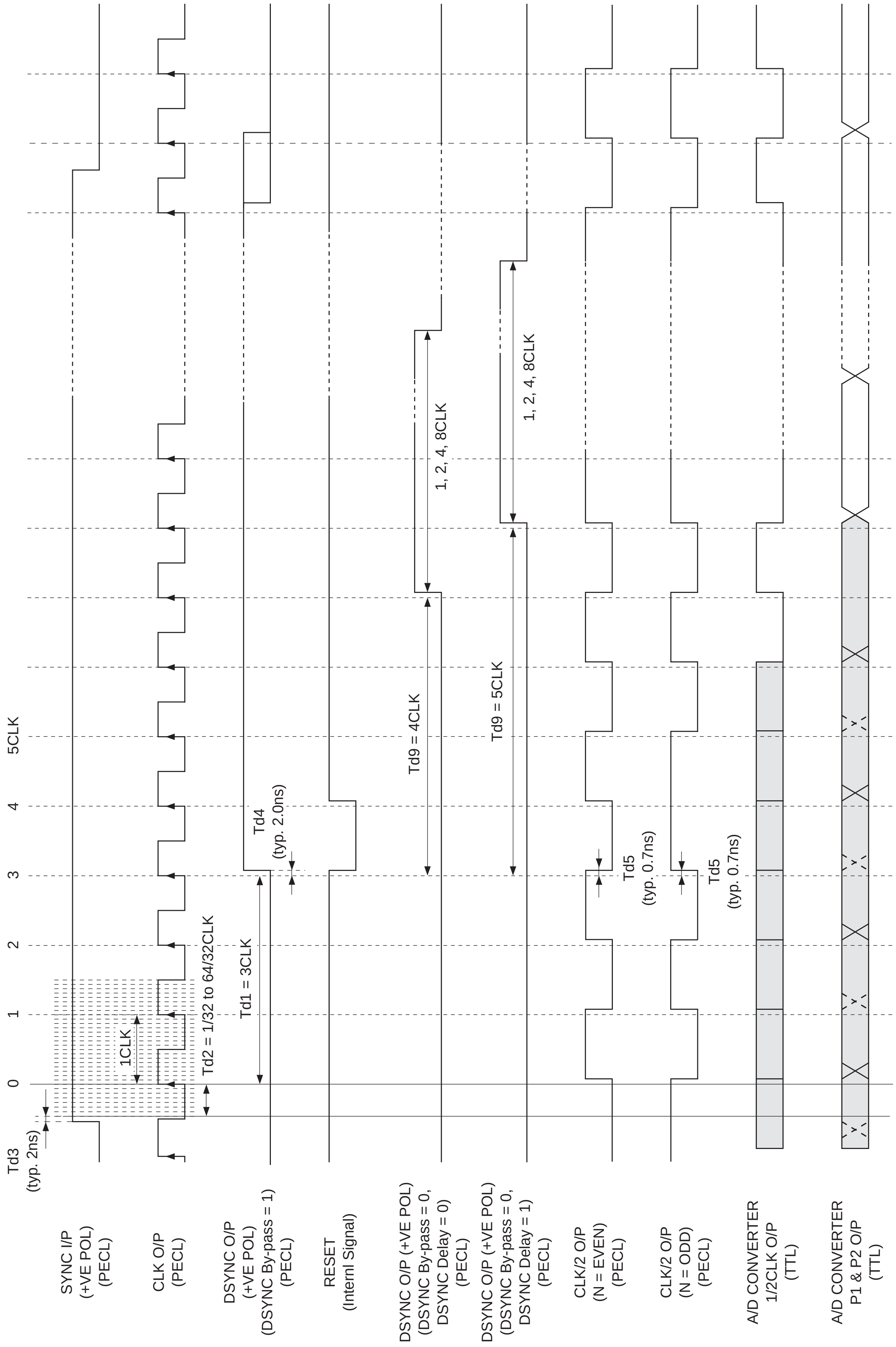


Timing Chart during Read Mode

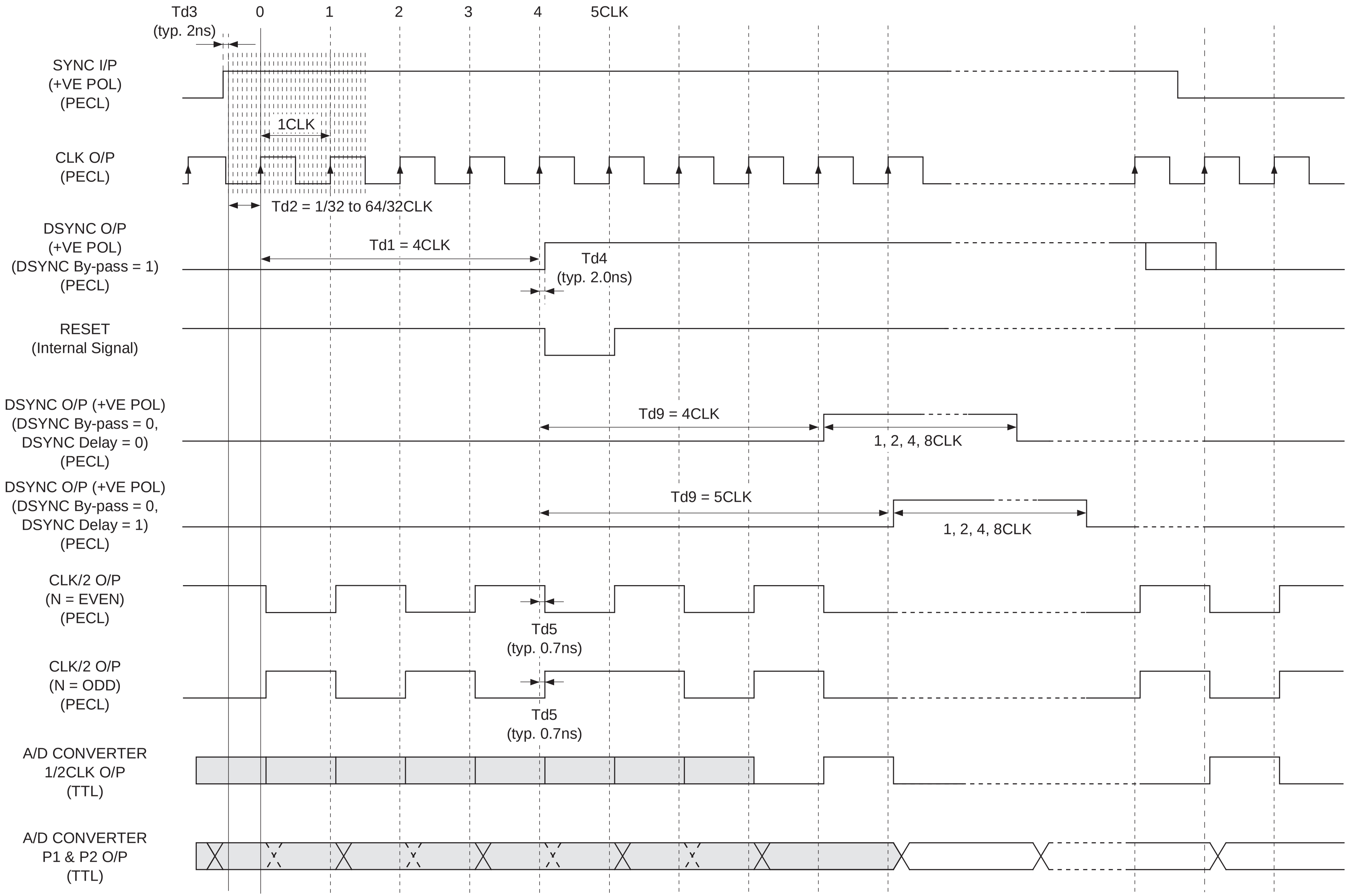
Timing Chart (Td1 = 2CLK)



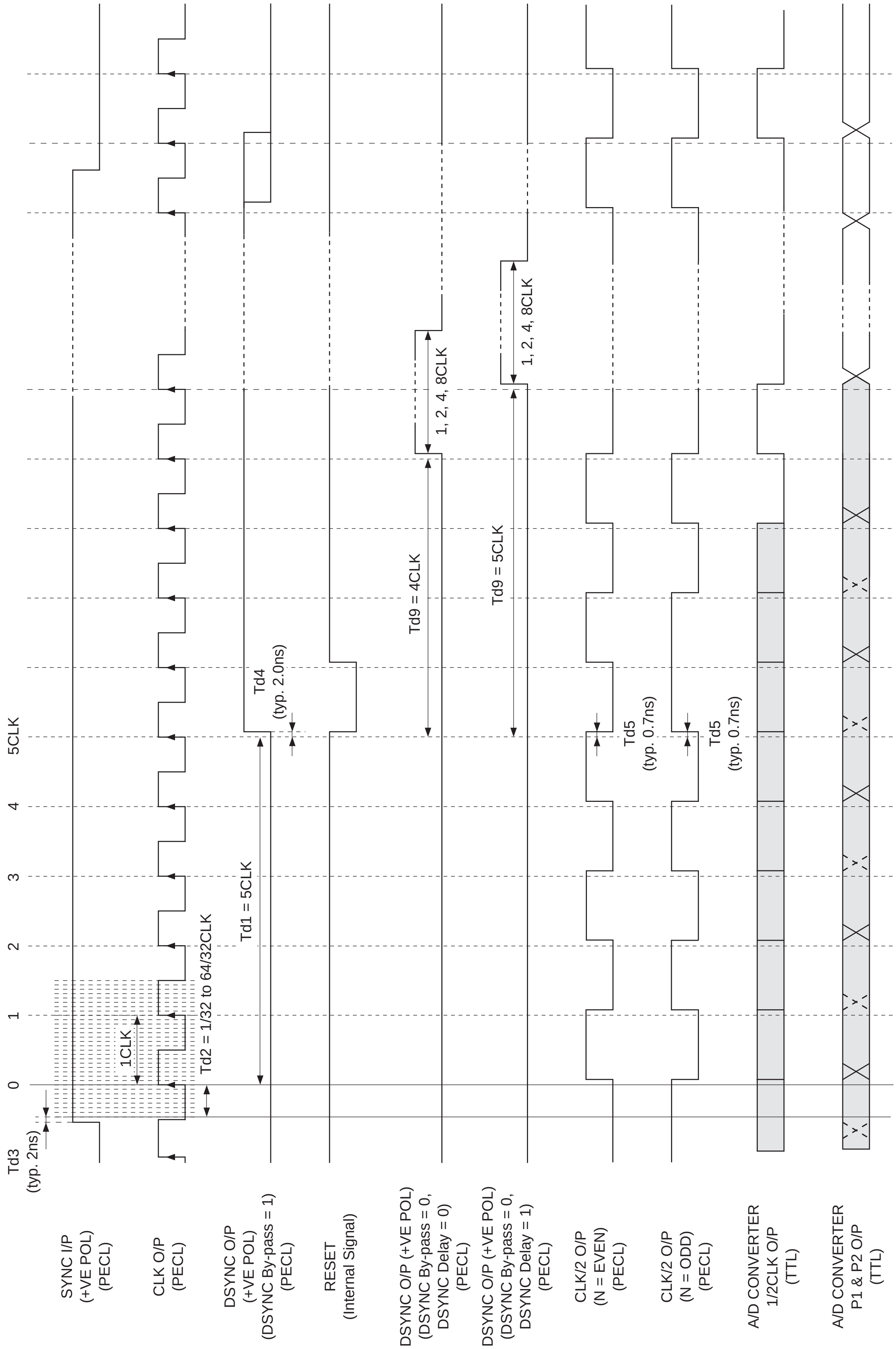
Timing Chart (Td1 = 3CLK)



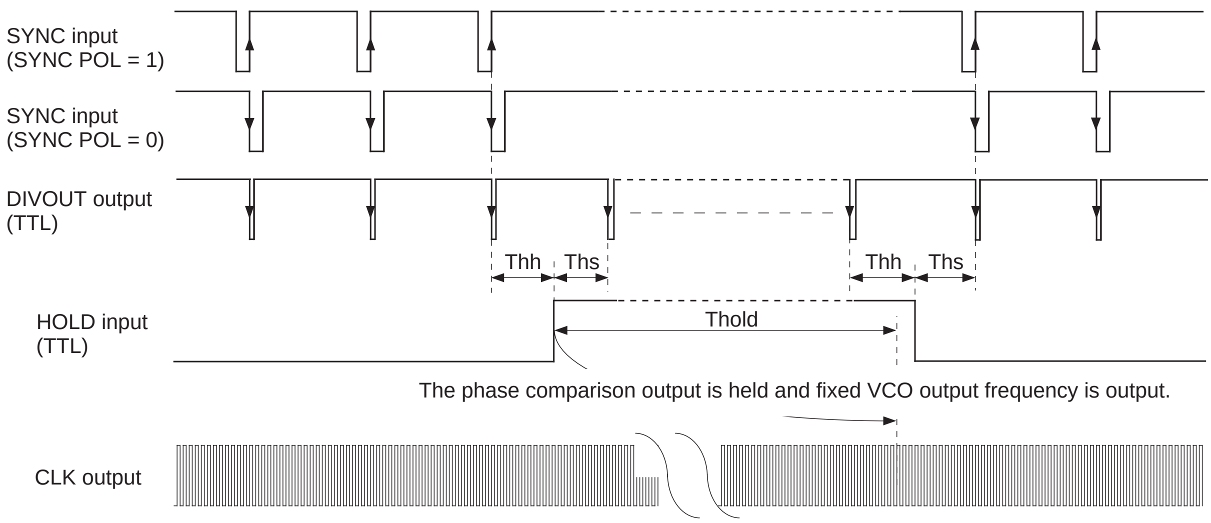
Timing Chart (Td1 = 4CLK)



Timing Chart (Td1 = 5CLK)

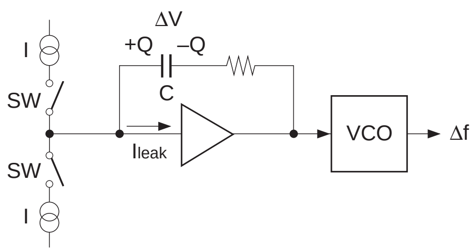


2. HOLD timing



HOLD signal set-up time (Ths) is a time from the rising edge of HOLD signal to the falling edge of DIVOUT. Or, when SYNC POL = 1, it is a time from the falling edge of HOLD signal to the rising edge of SYNC; when SYNC POL = 0, it is the time from the falling edge of HOLD signal to the falling edge of SYNC.
HOLD signal hold time (Thh) is the time from the falling edge of DIVOUT to falling edge of HOLD signal. Or, when SYNC POL = 1, it is the time from the rising edge of SYNC to the rising edge of HOLD signal; when SYNC POL = 0, it is the time from the falling edge of SYNC to the rising edge of HOLD signal.

When the HOLD input is held, the CLK frequency fluctuation can be calculated as follows.



$C \cdot \Delta V = Q = I_{leak} \cdot T_{hold}$

C: Loop filter capacitance
ΔV: Voltage variation due to leak current
I_{leak}: Internal amplifier leak current
T_{hold}: Hold time

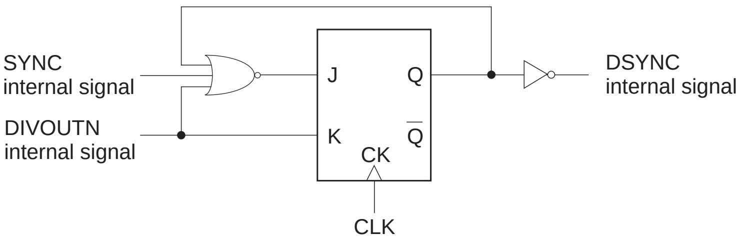
$\Delta V = I_{leak} \cdot T_{hold}/C$
$\Delta f = \Delta V \cdot KVCO = I_{leak} \cdot T_{hold}/C \cdot KVCO$

For example, assuming f = 100MHz, I_{leak} = 1nA, T_{hold} = 1ms, C = 0.068μF, and KVCO = 2π · 75MHz, then:

$\Delta V = 1 \times 10^{-9} \cdot 1 \times 10^{-3}/(0.068 \times 10^{-6}) = 15 \times 10^{-6}$ [V]

$\Delta f = 1 \times 10^{-9} \cdot 1 \times 10^{-3}/(0.068 \times 10^{-6}) \cdot 75 \times 10^{6} = 1125$ [Hz]

3. Relationship between SYNC input and DSYNC output during HOLD

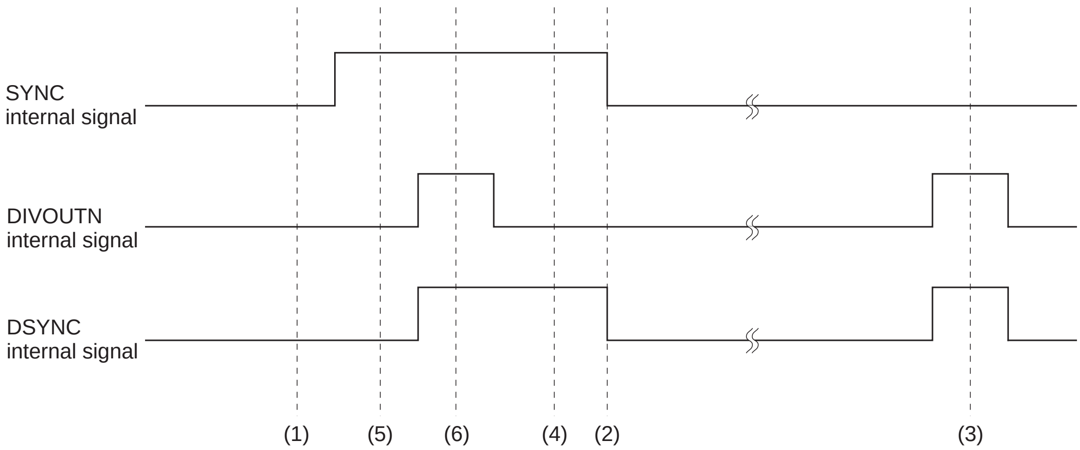


When the above SYNC internal and DIVOUTN internal signals are input, the DSYNC internal signal is output as shown in the table below.

1. DSYNC = L when SYNC = L and DIVOUTN = L.
2. DSYNC = H* or L* (unchanged with the previous data) when SYNC = H and DIVOUTN = L.
3. DSYNC = H when DIVOUTN = H (SYNC = H or L)

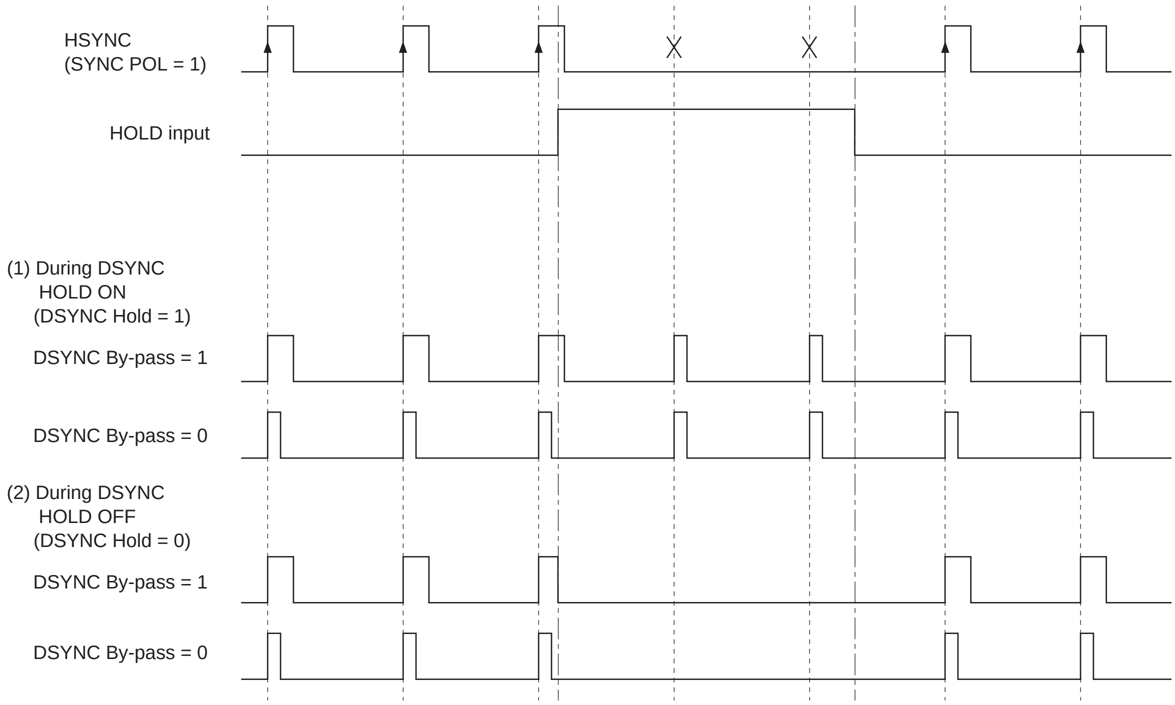
SYNC	DIVOUTN	J	K	Q	$\overline{Q}$	DSYNC	
L	L	L	L	L *	L *	L *	(1)
		H	L	H	L	L	(2)
L	H	L	H	L	H	H	(3)
H	L	L	L	L *	H *	H *	(4)
		L	L	H *	L *	L *	(5)
H	H	L	H	L	H	H	(6)

(*) is unchanged with the previous data.

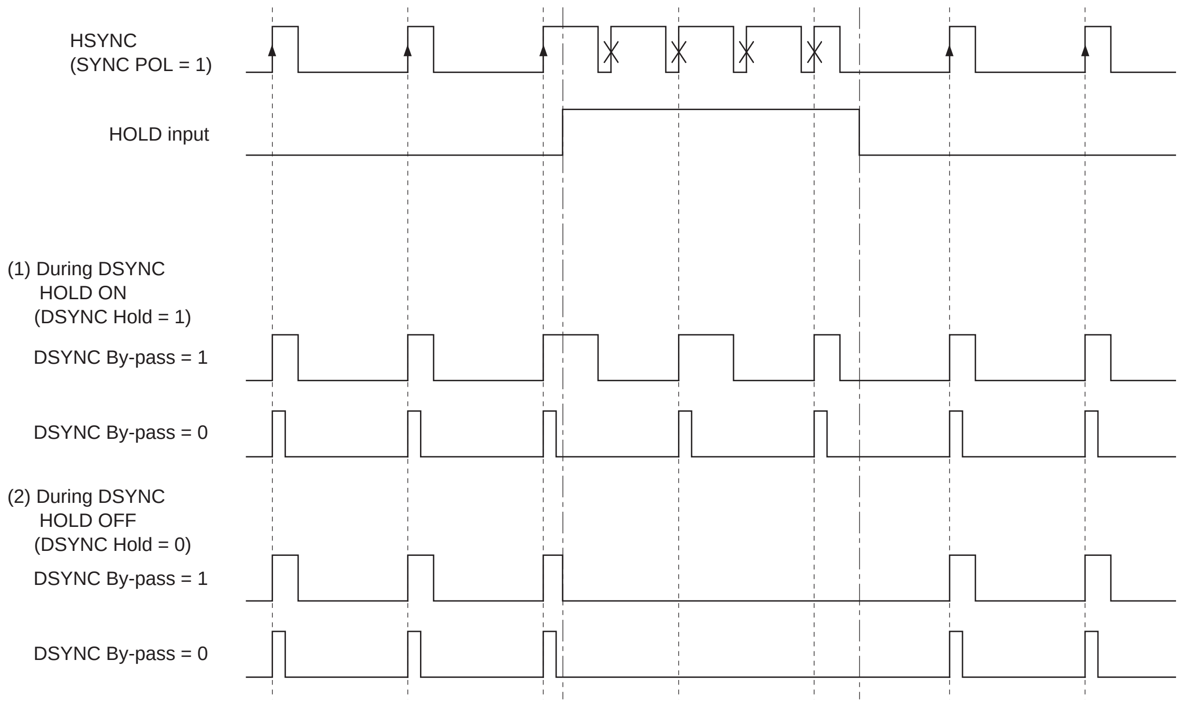


During HOLD, the output from DSYNC can be controlled by register DSYNC hold. Its output status differs according to the DSYNC polarity or DSYNC By-pass switching. The below diagrams show the relationship with DSYNC output for each SYNC input.
(DSYNC POL = 1 for all of CASE1 to CASE3.)

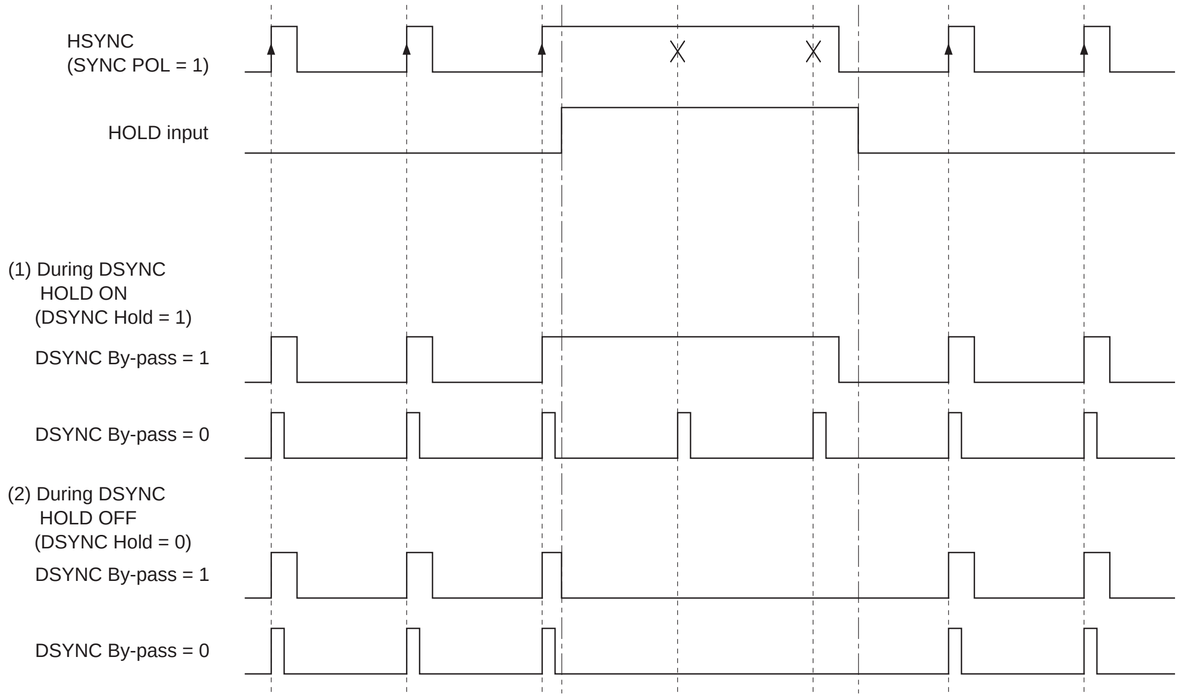
CASE1



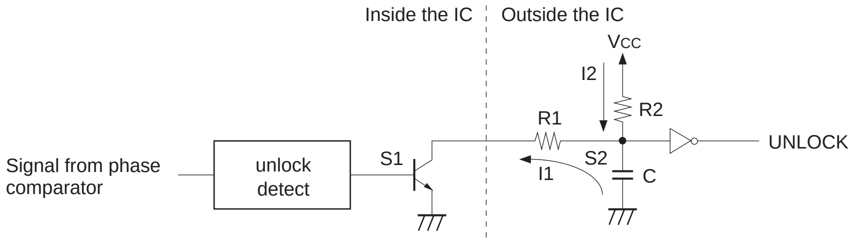
CASE2



CASE3

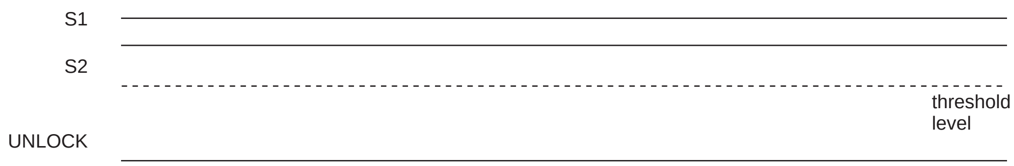

HSYNC
(SYNC POL = 1)
HOLD input
(1) During DSYNC
HOLD ON
(DSYNC Hold = 1)
DSYNC By-pass = 1
DSYNC By-pass = 0
(2) During DSYNC
HOLD OFF
(DSYNC Hold = 0)
DSYNC By-pass = 1
DSYNC By-pass = 0

4. UNLOCK timing

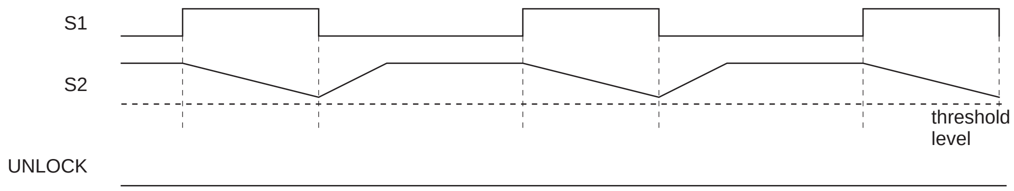


The unlock detect output is an open collector. When unlock detect output S1 goes high, the current I1 is pulled in. The UNLOCK sensitivity can be adjusted by connecting external resistors (R1, R2) and a capacitor (C) to this output pin appropriately and changing these values. Operation during three modes is described below.

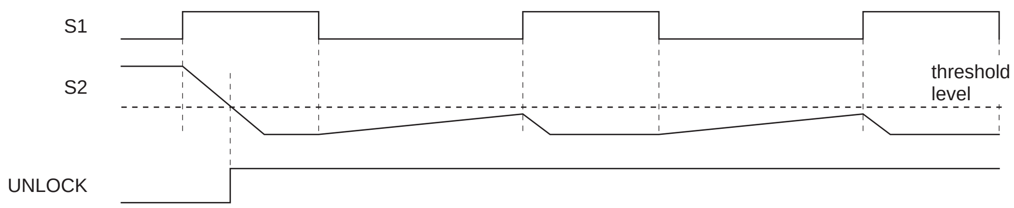
CASE 1: When there is no phase difference, that is to say, when the PLL is locked.
The S1 signal is low and the S2 signal is high.
The UNLOCK output remains low.



CASE 2: When there is a phase difference, that is to say, when the S1 signal goes high and low as shown in the figure below, the fall slew rate of the S2 signal is determined by the current I1 flowing into that open collector. Therefore, increasing the resistance R1 causes the S2 signal fall slew rate to become slower. Also, since the S2 signal rise slew rate is determined by the current I2, reducing the resistance R2 causes the S2 signal rise slew rate to become faster. If this integrated S2 signal does not fall below the threshold level of the next inverter, the UNLOCK signal stays low, and the PLL is said to be locked.

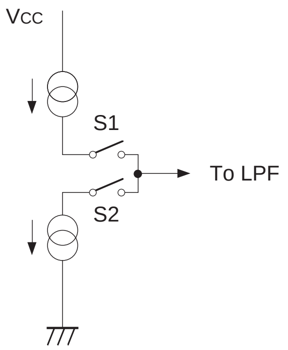


CASE 3: However, even if a phase difference exists as shown above, if the resistance R1 is reduced, the current I1 flowing into the open collector increases, and the S2 signal fall slew rate becomes faster. Also, if the resistance R2 is increased, the S2 signal rise slew rate becomes slower. If this integrated S2 signal falls below the threshold level of the next inverter, the UNLOCK signal goes from low to high, and the PLL is said to be unlocked.

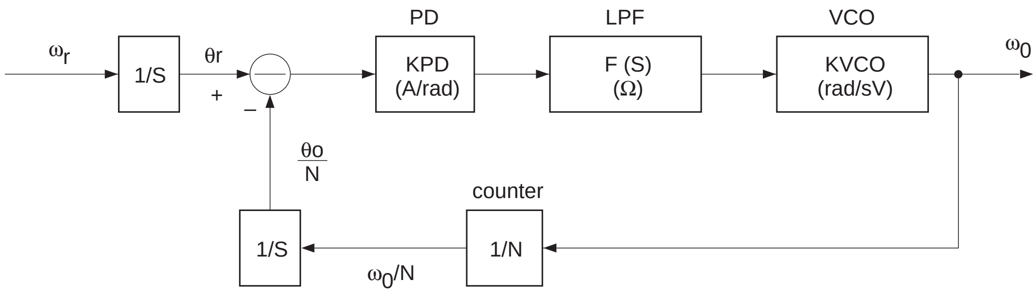


Charge Pump and Loop Filter Settings

The CXA3266Q's charge pump is a constant-current output type as shown below.



When a constant-current output charge pump circuit is used inside the PLL, the phase detector output acts as a current source, and the dimension of its transmittance KPD is A/rad. Also, when considering the VCO input as a voltage, the LPF transmittance dimension must be expressed in ohms (Ω = V/A).
Therefore, the PLL transmittance when a constant-current output charge pump circuit is used is as follows.



The PLL closed loop transmittance is obtained by the following formula.

$$\frac{\theta o/N}{\theta r} = \frac{KPD \cdot F(S) \cdot KVCO \cdot 1/N \cdot 1/S}{1 + KPD \cdot F(S) \cdot KVCO \cdot 1/N \cdot 1/S} \quad \text{... (1)}$$

Here, KPD, F (S), and KVCO are:

KPD:	Phase comparator gain	(A/rad)
F (S):	Loop filter transmittance	(Ω)
KVCO:	VCO gain	(rad/sV)

*1 The reason for the 1/S inside the phase detector is as follows.

$\theta o(t)/N = \int_0^t \omega_0(t)/N dt + \theta o(t = 0)/N$ ... (a)

If $\theta o(t = 0) = 0$,

$\theta o(t)/N = \int_0^t \omega_0(t)/N dt$ ... (b)

Performing Laplace conversion:

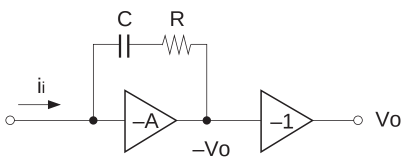
$\theta o(S)/N = \frac{1}{s} W_0(S)/N$ ... (c)

The loop filter F (s) is described below.

The loop filter smoothes the output pulse from the phase comparator and inputs it as the DC component to the VCO. In addition to this, however, the loop filter also plays an important element in determining the PLL response characteristics.

Typical examples of loop filters include lag filters, lag-lead filters, active filters, etc. However, the CXA3266Q's LPF is a current input type active filter as shown below, so the following calculations show an actual example of deriving the PLL closed loop transmittance when using this type of filter and then using this transmittance to create a formula for setting the filter constants.

Current input type active filter



The filter transmittance is as follows.

$$\frac{VO}{A} + VO = (R + \frac{1}{SC})$$

$$F(S) = \frac{1 + SRC}{SC} \cdot \frac{A}{1 + A}$$

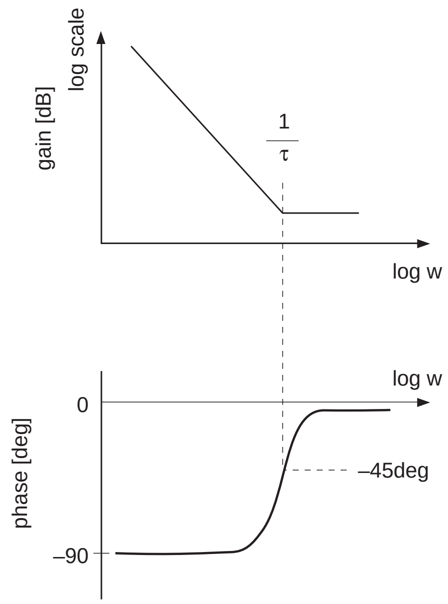
$$= \frac{1 + S\tau}{SC} \cdot \frac{A}{1 + A}$$

$$\therefore \tau = RC$$

Here, assuming A > 1, then:

$$F(S) = \frac{1 + S\tau}{SC} \quad \cdots\cdots\cdots (2)$$

The Bode diagram for formula (2) is as follows.



Next, substituting (2) into (1) and obtaining the overall closed loop transmittance for the PLL:

$$\frac{\theta o/N}{\theta r} = \frac{\frac{KPD \cdot KVCO \cdot \tau}{NC} \cdot S + \frac{KPD \cdot KVCO}{NC}}{S^2 + \frac{KPD \cdot KVCO \cdot \tau}{NC} \cdot S + \frac{KPD \cdot KVCO}{NC}} \quad \cdots (3)$$

$$= \frac{2\zeta\omega nS + \omega n^2}{S^2 + 2\zeta\omega nS + \omega n^2} \quad \cdots\cdots\cdots (4)$$

$$\omega n = \sqrt{\frac{KPD \cdot KVCO}{NC}} \quad \cdots\cdots\cdots (5)$$

$$\zeta = \frac{1}{2} \omega n\tau \quad \cdots\cdots\cdots (6)$$

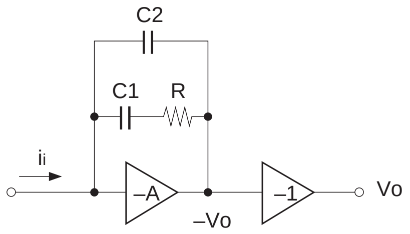
Here, ωn and ζ are as follows.

ωn characteristic angular frequency:
The oscillatory angular frequency when PLL oscillation is assumed to have been maintained by the loop filter and individual loop gains is called the characteristic angular frequency: ωn.

ζ damping factor:
This is the PLL transient response characteristic, and serves as a measure of the PLL stability. It is determined by the loop gain and the loop filter.

A capacitor C2 is added to the actual loop filter.
This added capacitor C2 is used to reduce the R noise, and a value of around 1/10 to 1/1000 of C1 should be selected as necessary.

Current input type active filter with added capacitor C2



The filter transmittance is as follows.

$$F(S) = \frac{1 + C1 \cdot R \cdot S}{S((C1 + C2) + C1 \cdot C2 \cdot R \cdot S)}$$

$$= \frac{1 + \tau_1 \cdot S}{S(C1 + C2)(1 + \tau_2 \cdot S)} \quad \cdots\cdots\cdots\cdots\cdots (7)$$

$$\tau_1 = C1 \cdot R$$

$$\tau_2 = \frac{C1 \cdot C2 \cdot R}{C1 + C2}$$

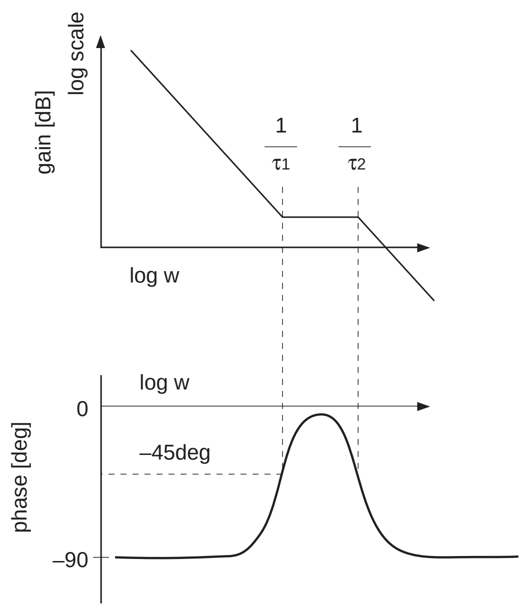
Here, assuming C2 = C1/100, then:

$$\tau_2 = \frac{C1 \cdot C1/100 \cdot R}{C1 + C1/100}$$

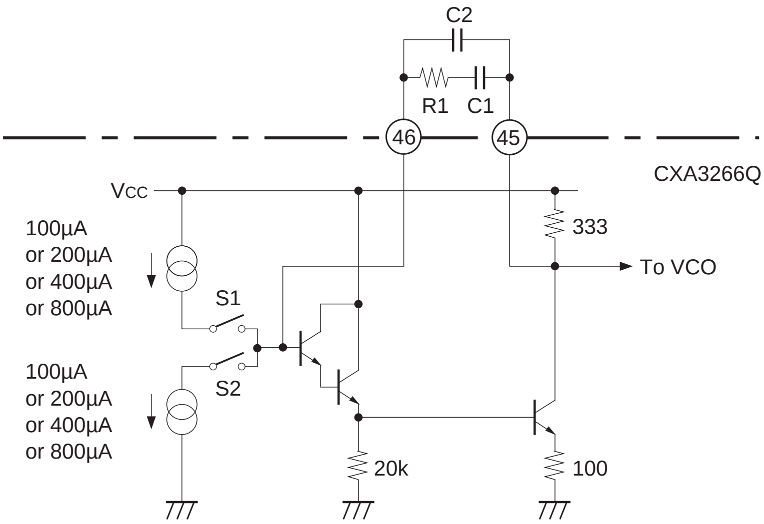
$$= \frac{1}{101} C1 \cdot R$$

$$= \frac{1}{101} \tau_1$$

The Bode diagram for formula (7) is as follows.



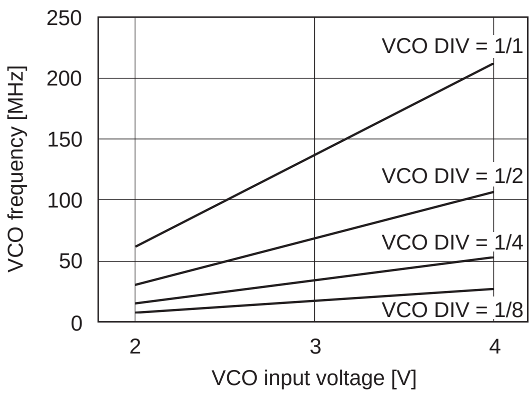
Next, the various parameters inside an actual CXA3266Q are obtained.
The CXA3266Q's charge pump output block and the LPF circuit are as follows.



First, KPD is as follows.

KPD = 100µ/2π or 200µ/2π or 400µ/2π or 800µ/2 π (A/rad)

Typical KVCO characteristics curves for the CXA3266Q's internal VCO are as follows.



Therefore, KVCO is as follows.

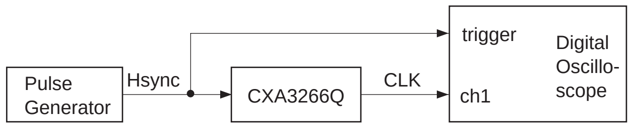
KVCO = 2π · 75M or 2π · 37.5M or 2π · 18.75M or 2π · 9.375M (rad/sV) ωn and ζ calculated for various types of computer signals are shown below.

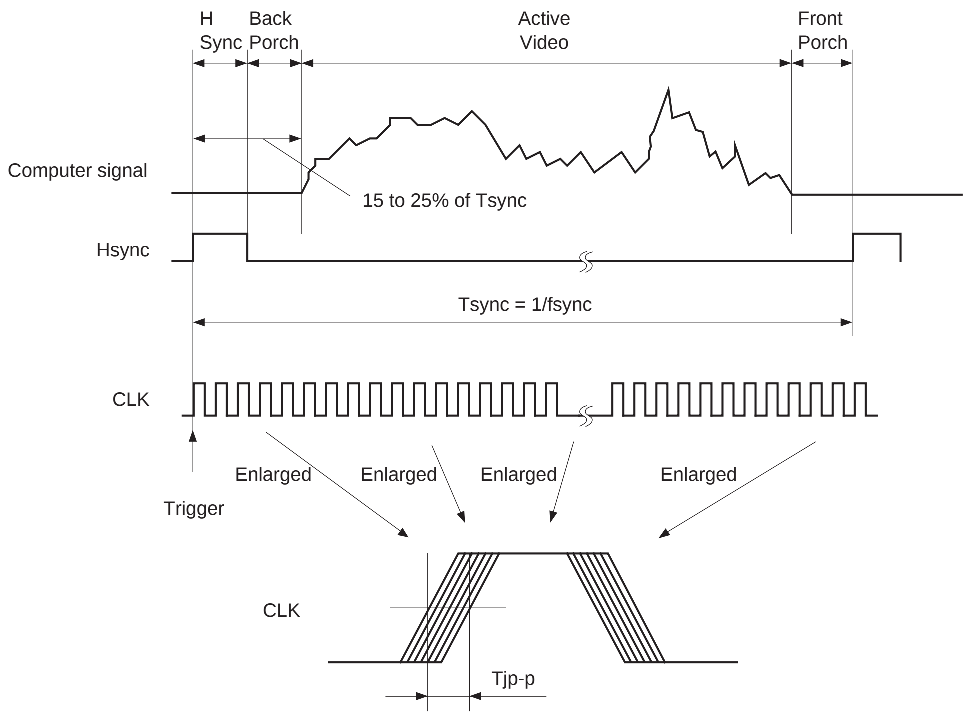
Here, the various parameters are as follows.
FSYNC: Input H sync frequency
FCLK: Output clock frequency
KPD × 2π: Phase comparator gain × 2π (KPD × 2π = +100 or 200 or 400 or 800)
KVCO/2π: VCO gain (when VCO DIV = 1/1, KVCO/2π = 75)
(when VCO DIV = 1/2, KVCO/2π = 75/2)
(when VCO DIV = 1/4, KVCO/2π = 75/4)
(when VCO DIV = 1/8, KVCO/2π = 75/8)
N: Counter value
C1: Loop filter capacitance value
R1: Loop filter resistance value

MODE	Resolution	HSYNC	FCLK	KPD × 2π	C.Pump setting		KVCO/2π	DIV1, 2, 4, 8 setting		N setting	C1	R1	ωn	fn	ζ
		kHz	MHz	µA	Bit1	Bit0	M/(S × V)	Bit1	Bit0		µF	kΩ	kHzrad	kHz	
NTSC		15.73	12.27	400	1	0	75/8	1	1	780	0.068	3.0	8.41	1.34	0.86
NTSC		15.73	18.41	400	1	0	75/8	1	1	1170	0.068	3.0	6.87	1.09	0.70
NTSC		15.73	24.55	800	1	1	75/8	1	1	1560	0.068	3.0	8.41	1.34	0.86
PAL		15.63	14.69	400	1	0	75/8	1	1	940	0.068	3.0	7.66	1.22	0.78
PAL		15.63	22.03	800	1	1	75/8	1	1	1410	0.068	3.0	8.84	1.41	0.90
PAL		15.63	29.38	400	1	0	75/4	1	0	1880	0.068	3.0	7.66	1.22	0.78
PC-98	640 × 480	24.82	21.05	400	1	0	75/8	1	1	848	0.068	3.0	8.06	1.28	0.82
VGA	640 × 480	31.47	25.18	400	1	0	75/8	1	1	800	0.068	3.0	8.30	1.32	0.85
MAC	640 × 480	35.00	30.24	400	1	0	75/4	1	0	864	0.068	3.0	11.30	1.80	1.15
VESA	640 × 480	37.86	31.50	400	1	0	75/4	1	0	832	0.068	3.0	11.51	1.83	1.17
SVGA	800 × 600	35.16	36.00	400	1	0	75/4	1	0	1024	0.068	3.0	10.38	1.65	1.06
SVGA	800 × 600	37.88	40.00	400	1	0	75/4	1	0	1056	0.068	3.0	10.22	1.63	1.04
SVGA	800 × 600	46.88	49.51	400	1	0	75/4	1	0	1056	0.068	3.0	10.22	1.63	1.04
SVGA	800 × 600	48.08	50.00	400	1	0	75/4	1	0	1040	0.068	3.0	10.30	1.64	1.05
SVGA	800 × 600	53.67	56.25	400	1	0	75/2	0	1	1048	0.068	3.0	14.51	2.31	1.48
MAC	832 × 624	49.72	57.28	400	1	0	75/2	0	1	1152	0.068	3.0	13.84	2.20	1.41
XGA	1024 × 768	48.36	65.00	400	1	0	75/2	0	1	1344	0.068	3.0	12.81	2.04	1.31
XGA	1024 × 768	56.48	75.01	400	1	0	75/2	0	1	1328	0.068	3.0	12.89	2.05	1.31
XGA	1024 × 768	60.02	78.75	400	1	0	75/2	0	1	1312	0.068	3.0	12.97	2.06	1.32
MAC	1024 × 768	60.24	80.00	400	1	0	75/2	0	1	1328	0.068	3.0	12.89	2.05	1.31
XGA	1024 × 768	68.68	94.50	400	1	0	75/2	0	1	1376	0.068	3.0	12.66	2.02	1.29
SXGA	1280 × 1024	46.43	78.75	400	1	0	75/2	0	1	1696	0.068	3.0	11.40	1.82	1.16
SXGA	1280 × 1024	63.98	108.00	400	1	0	75/1	0	0	1688	0.068	3.0	16.17	2.57	1.65
SXGA	1280 × 1024	79.98	135.01	400	1	0	75/1	0	0	1688	0.068	3.0	16.17	2.57	1.65
SXGA	1280 × 1024	91.15	156.96	400	1	0	75/1	0	0	1722	0.068	3.0	16.01	2.55	1.63
UXGA	1600 × 1200	81.23	175.46	800	1	1	75/1	0	0	2160	0.068	3.0	20.21	3.22	2.06
UXGA	1600 × 1200	93.72	202.44	800	1	1	75/1	0	0	2160	0.068	3.0	20.21	3.22	2.06

CLK Jitter Evaluation Method

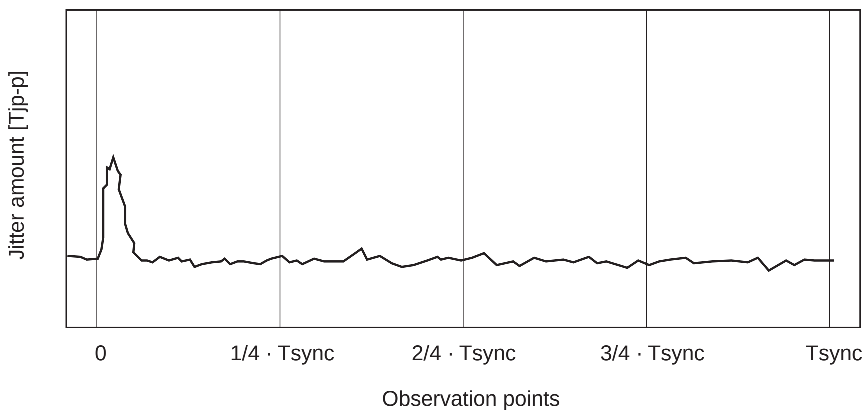
The regenerated CLK is obtained by applying Hsync to the CXA3266Q. Apply this CLK to a digital oscilloscope and observe the CLK waveform using Hsync as the trigger.



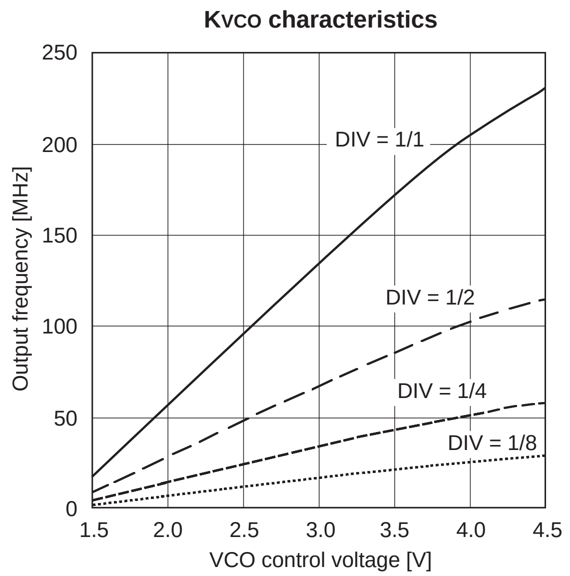


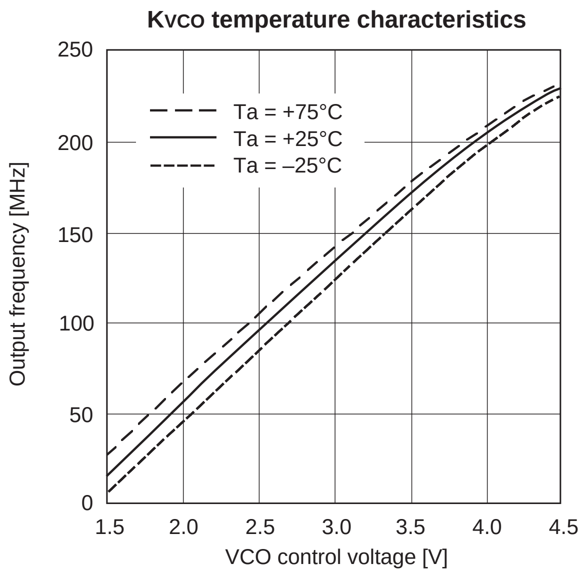
The CLK jitter is measured at peak to peak in the long-term write mode of the digital oscilloscope as shown in the figure. The CLK jitter size varies according to the difference in the relative position with respect to Hsync. Therefore, when the observation point is changed, the CLK jitter at that point is observed.

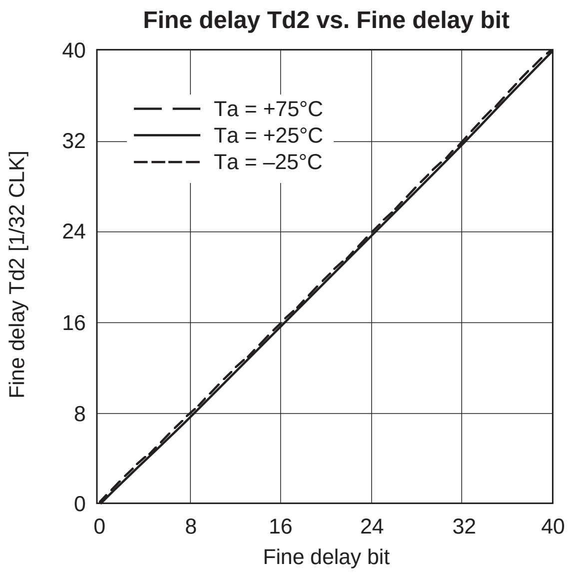
The figure below shows an typical example of the CLK jitter for the CXA3266Q.
The CLK jitter increases slightly at the rising edge of Hsync (in the case of positive polarity), and then settles down thereafter. However, this is not a problem as the active pixels start after about 20% of the H cycle has passed from the rising edge of Hsync.



Example of Representative Characteristics





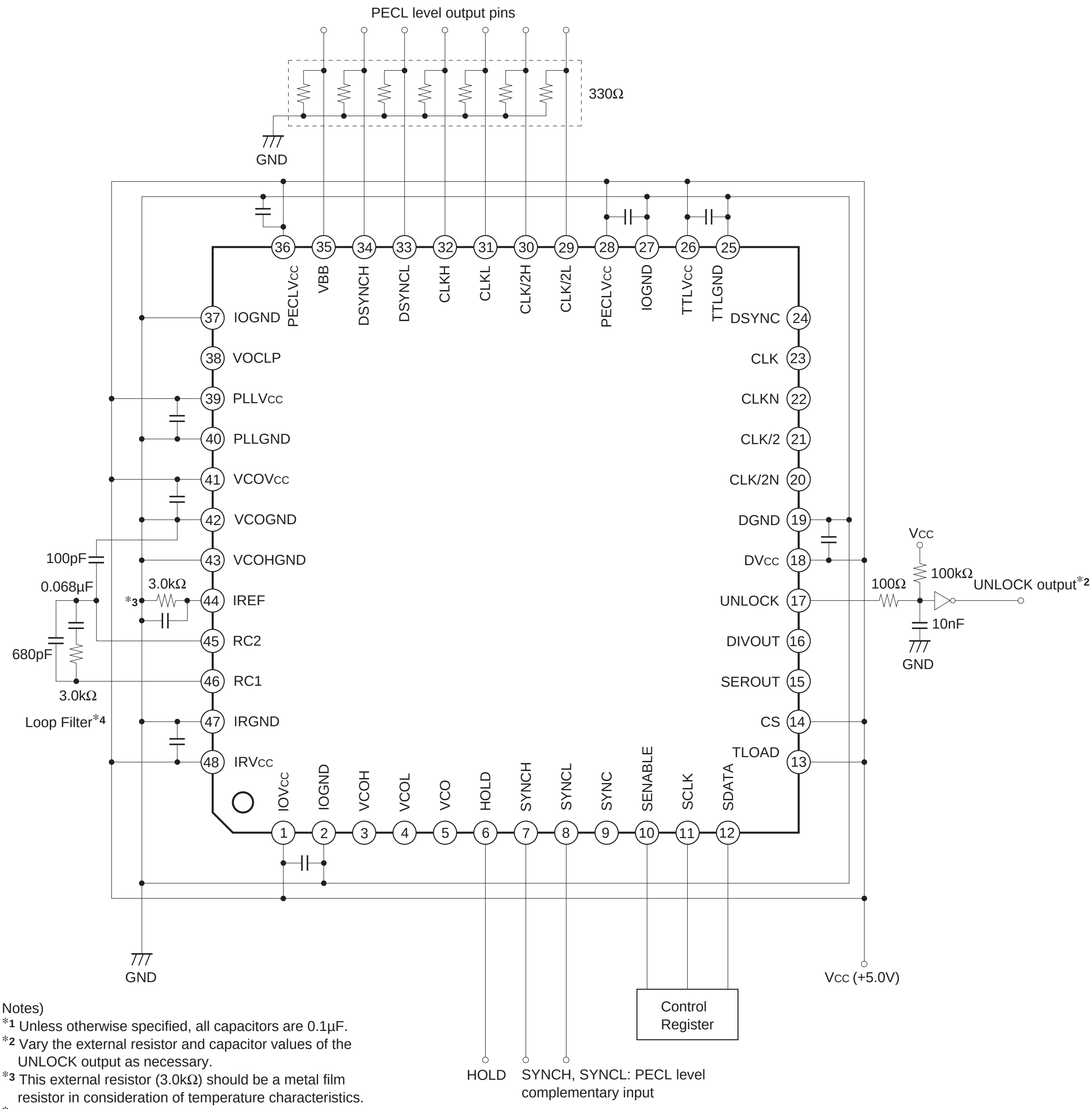


Notes on Operation

- Be sure not to separate the analog and digital power supplies, and the analog and digital GND.
- The ground pattern should be as wide as possible. Using a multi-layer substrate with a mat ground is recommended.
- Ground the power supply pins of the IC with a 0.1µF or larger ceramic chip capacitor as close to each pin as possible.
- Be sure to accurately match the I/O characteristic impedance in order to ensure sufficient performance during high-speed operation.
- Design the set so that the loop filter (external) is located at the minimum distance. (See the CXA3266Q PWB.)

(1) Recommended PECL I/O circuit

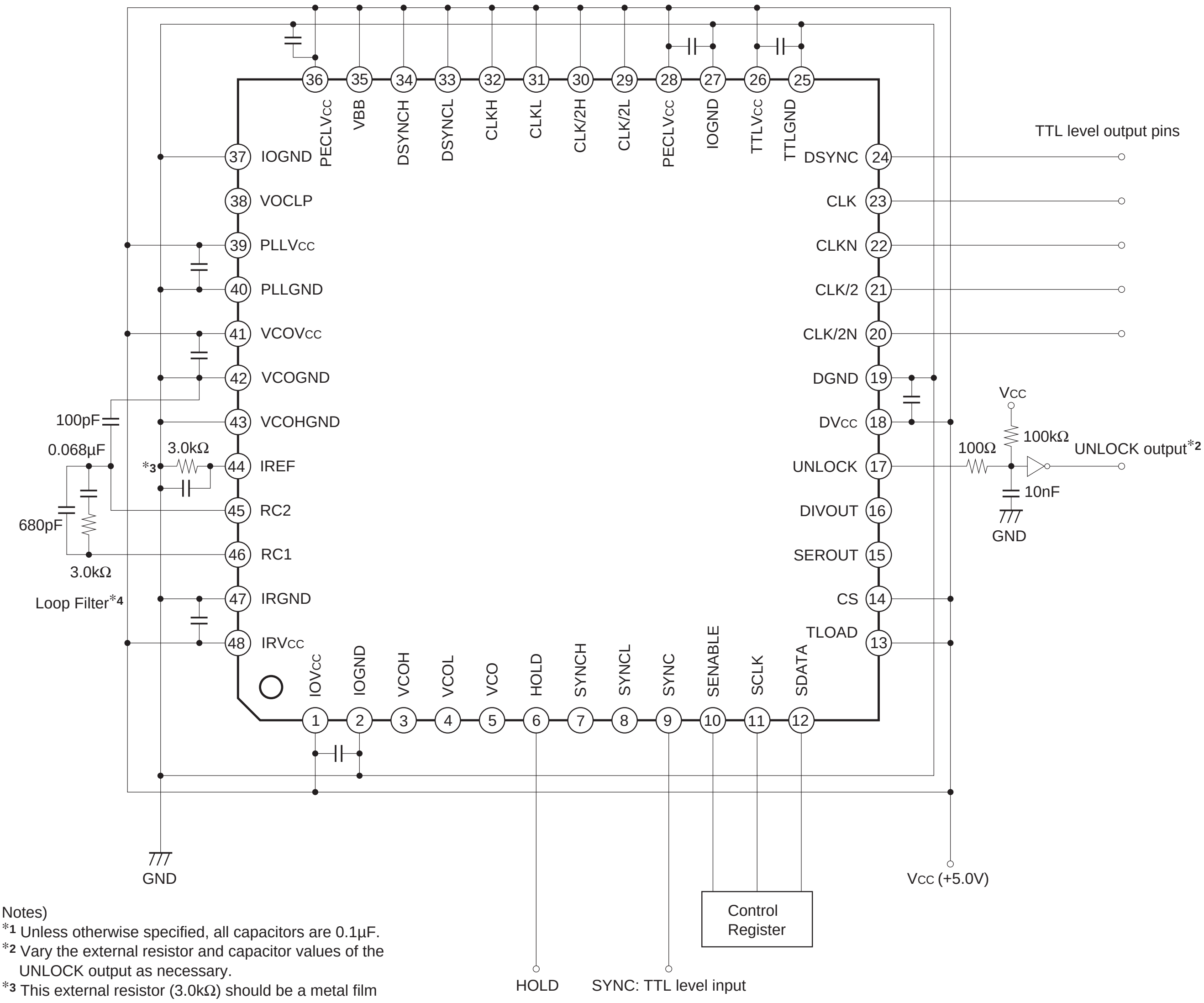
The peripheral circuits mainly use PECL for digital input and output. Of course, PECL and TTL can also be mixed. In this case, disable the TTL outputs with the control registers.



Notes)
*1 Unless otherwise specified, all capacitors are 0.1μF.
*2 Vary the external resistor and capacitor values of the UNLOCK output as necessary.
*3 This external resistor (3.0kΩ) should be a metal film resistor in consideration of temperature characteristics.
*4 The loop filter's capacitors and resistor should also be temperature compensated.

(2) Recommended TTL I/O circuit

The peripheral circuits mainly use TTL for digital input and output. Of course, PECL and TTL can also be mixed.

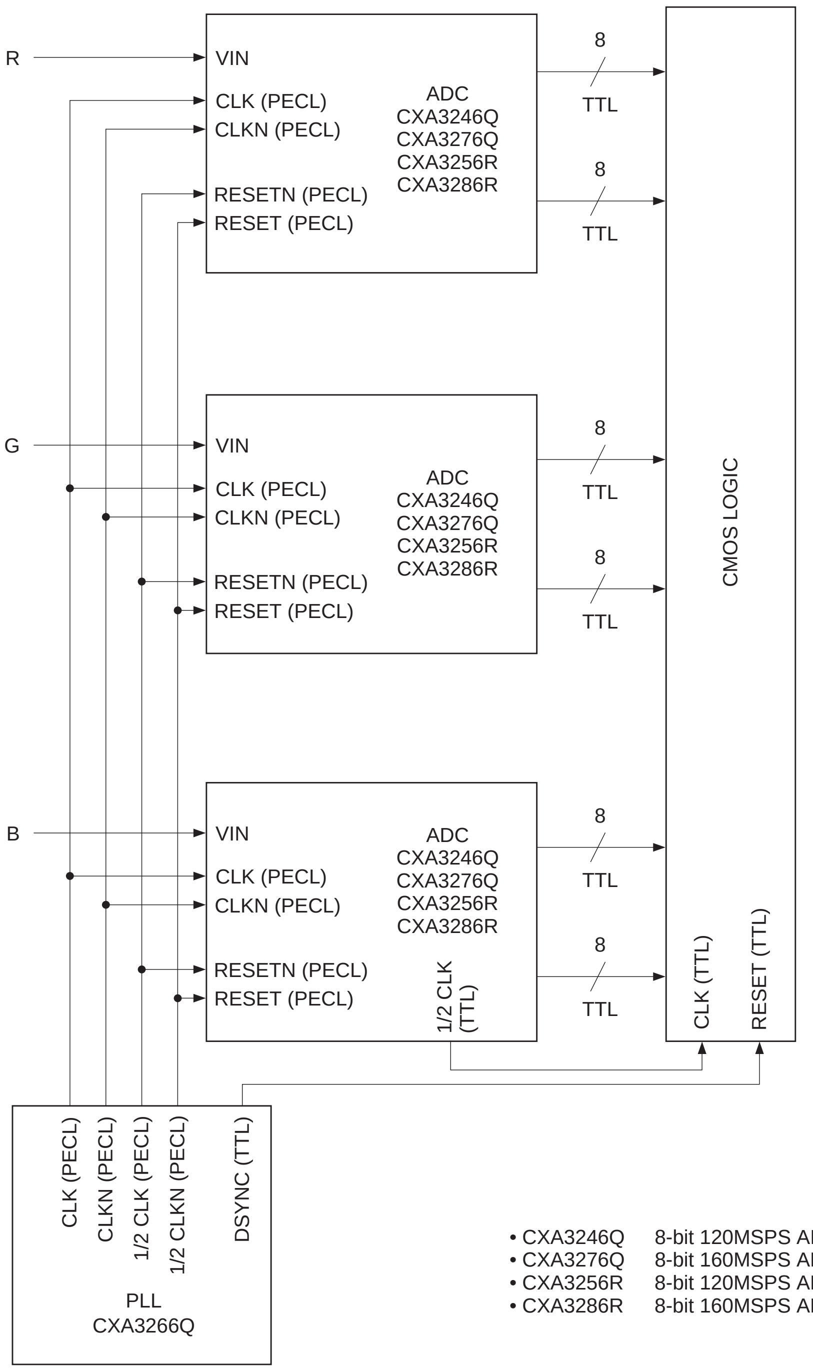


Notes)
*1 Unless otherwise specified, all capacitors are 0.1µF.
*2 Vary the external resistor and capacitor values of the UNLOCK output as necessary.
*3 This external resistor (3.0kΩ) should be a metal film resistor in consideration of temperature characteristics.
*4 The loop filter's capacitors and resistor should also be temperature compensated.

Connecting the CXA3266Q with Sony ADC (Demultiplex Mode)

When connecting the PLL output to A/D converters with built-in demultiplex function such as the CXA3246Q/CXA3276Q/CXA3256R/CXA3286R (Sony), a simple system can be configured by connecting the CLK (PECL) and CLKN (PECL) outputs of the CXA3266Q to the CLK (PECL) and CLKN (PECL) inputs of each A/D converter, respectively, and the 1/2 CLK (PECL) and 1/2 CLKN (PECL) outputs of the CXA3266Q to the RESETN (PECL) and RESET (PECL) inputs of each A/D converter, respectively (when the PLL counter value N is an even number).

Wiring Diagram



- CXA3246Q 8-bit 120MSPS ADC
- CXA3276Q 8-bit 160MSPS ADC
- CXA3256R 8-bit 120MSPS ADC
- CXA3286R 8-bit 160MSPS ADC

CXA3266Q and Sony ADC (Demultiplex Mode) Timing: 120MHz specification

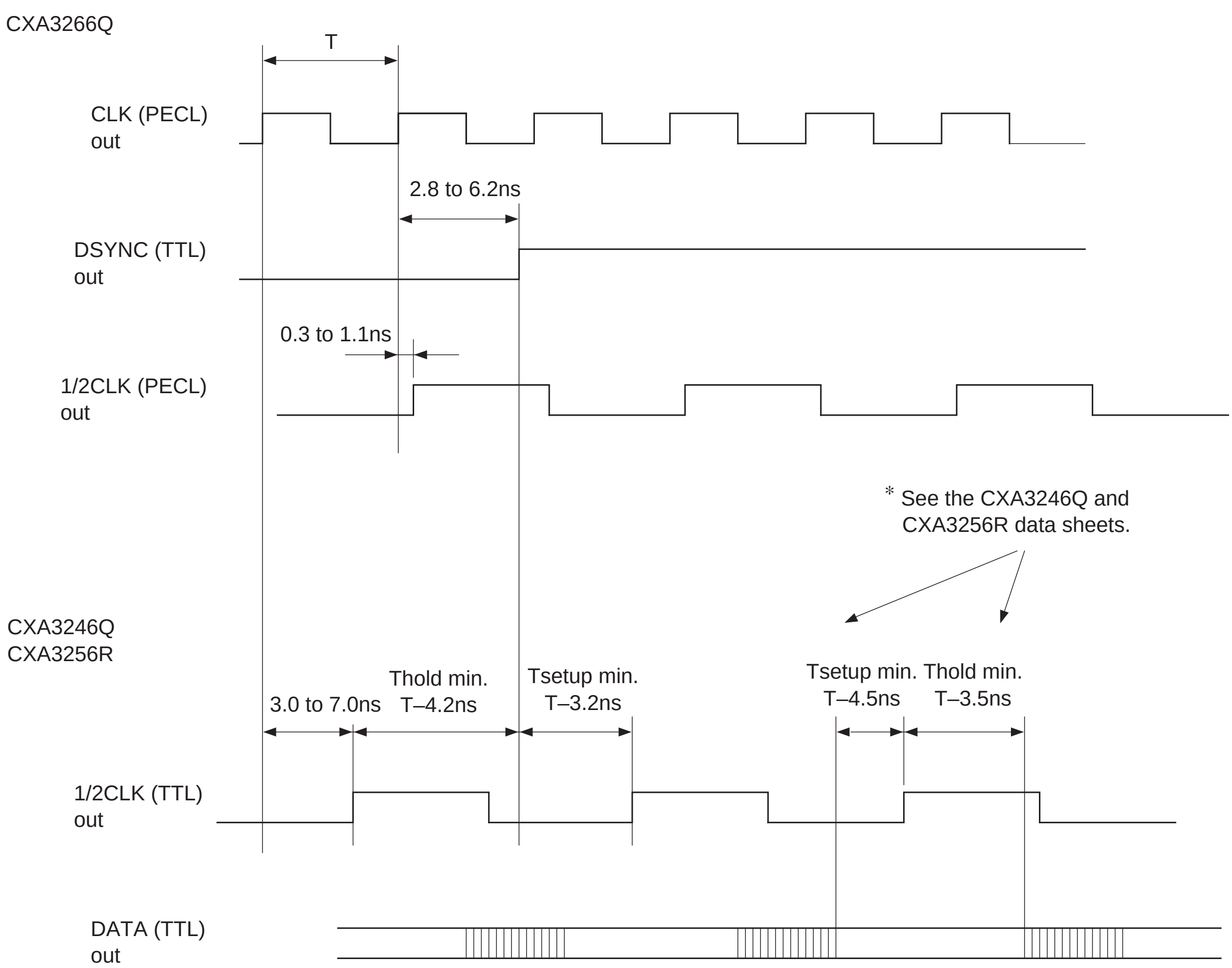
The CXA3266Q and CXA3246Q/CXA3256R timings are shown below.

Here, the important timings are as follows.
(The clock cycle is labeled as T.)

- For the A/D converters
  Clock input vs. reset input
  The set-up time is T–1.1ns and the hold time is 0.3ns, satisfying the A/D converter specifications.

- For the CMOS LOGIC at the rear end of the A/D converters
  A/D converter data output vs. 1/2 clock output timing
  The set-up time is T–4.5ns and the hold time is T–3.5ns. (These timings also include combinations of three A/D converters from different lots, and are defined for all operating temperatures and all operating supply voltages. See the CXA3246Q/CXA3256R data sheets for a detailed description.)

- For the CMOS LOGIC at the rear end of the A/D converters
  DSYNC signal from CXA3266Q vs. A/D converter 1/2 clock output
  The set-up time is T–3.2ns and the hold time is T–4.2ns.



CXA3266Q and Sony ADC (Demultiplex Mode) Timing: 160MHz specification

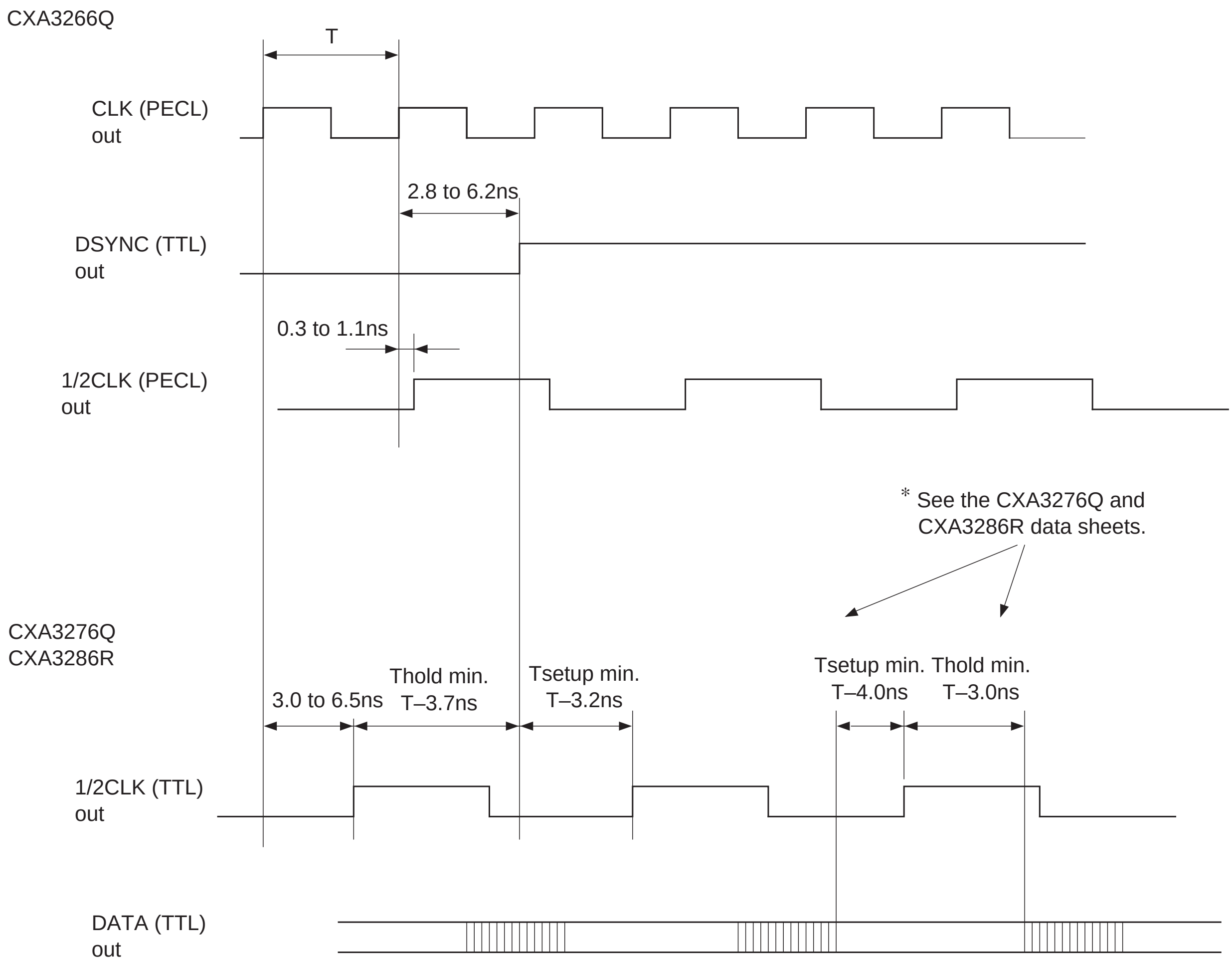
The CXA3266Q and CXA3276Q/CXA3286R timings are shown below.

Here, the important timings are as follows.
(The clock cycle is labeled as T.)

- For the A/D converters
  Clock input vs. reset input
  The set-up time is T–1.1ns and the hold time is 0.3ns, satisfying the A/D converter specifications.

- For the CMOS LOGIC at the rear end of the A/D converters
  A/D converter data output vs. 1/2 clock output timing
  The set-up time is T–4.0ns and the hold time is T–3.0ns. (These timings also include combinations of three A/D converters from different lots, and are defined for all operating temperatures and all operating supply voltages. See the CXA3276Q/CXA3286R data sheets for a detailed description.)

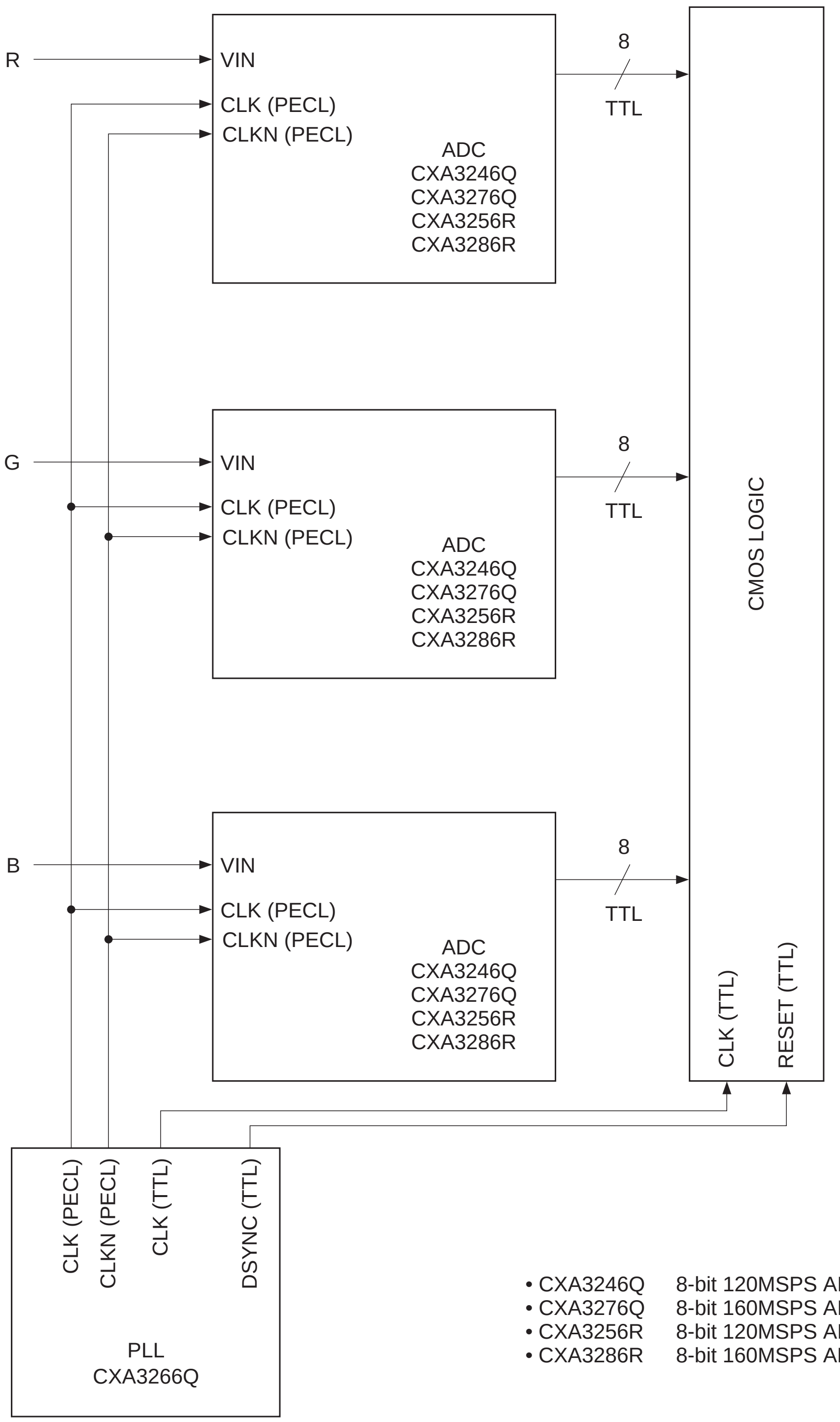
- For the CMOS LOGIC at the rear end of the A/D converters
  DSYNC signal from CXA3266Q vs. 1/2 clock output of A/D converter
  The set-up time is T–3.2ns and the hold time is T–3.7ns.



Connecting the CXA3266Q with Sony ADC (Straight Mode)

When connecting the PLL output to A/D converters such as the CXA3246Q/CXA3276Q/CXA3256R/CXA3286R (Sony), a simple system can be configured as shown below.

Wiring Diagram



- CXA3246Q 8-bit 120MSPS ADC
- CXA3276Q 8-bit 160MSPS ADC
- CXA3256R 8-bit 120MSPS ADC
- CXA3286R 8-bit 160MSPS ADC

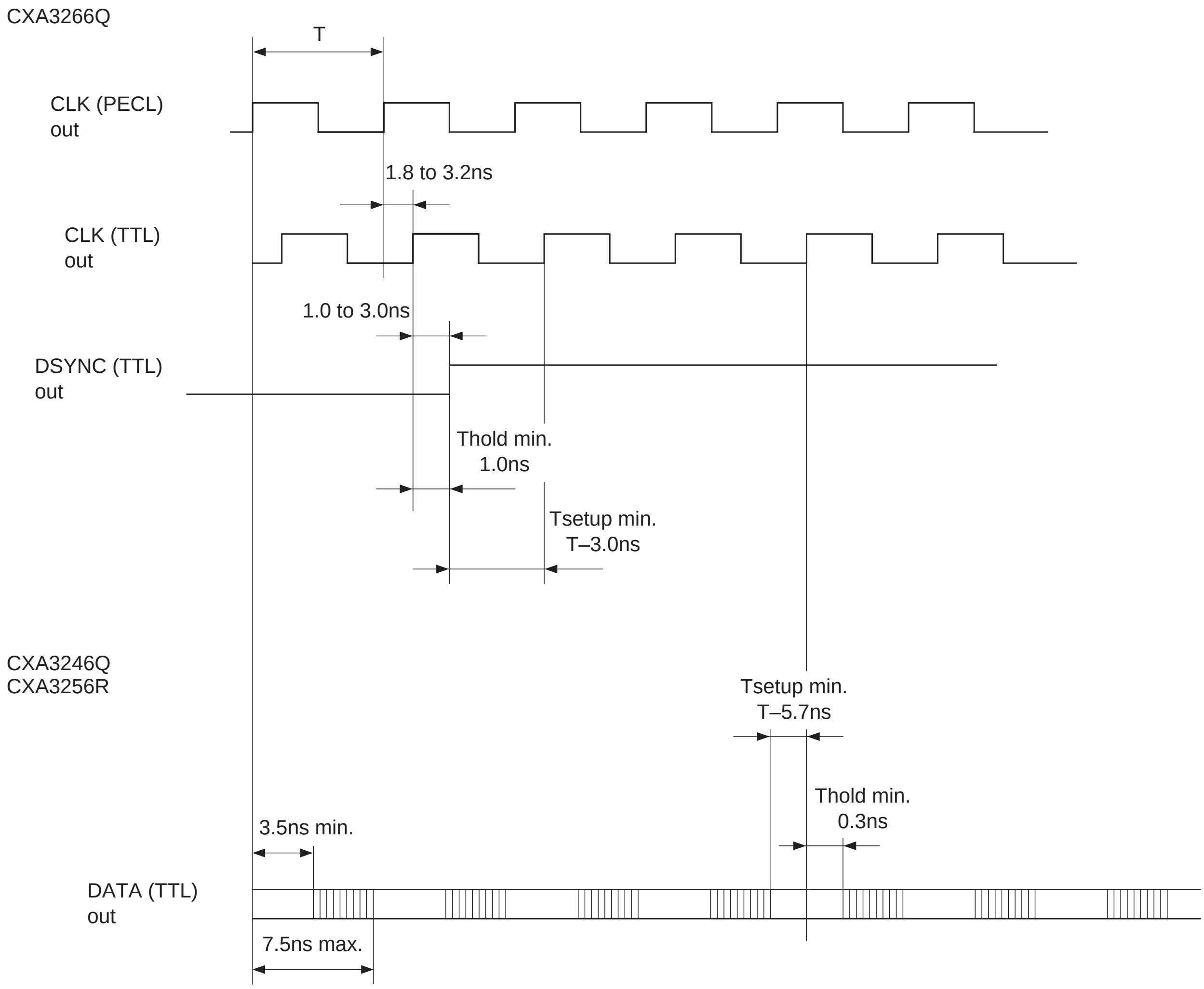
CXA3266Q and Sony ADC (Straight Mode) Timing: 100MHz specification

The CXA3266Q and CXA3246Q/CXA3256R timings are shown below.

Here, the important timings are as follows.
(The clock cycle is labeled as T.)

- For the CMOS LOGIC at the rear end of the A/D converters
  A/D converter data output vs. clock output from CXA3266Q
  The set-up time is T–5.7ns and the hold time is 0.3ns. (These timings also include combinations of three A/D converters from different lots, and are defined for all operating temperatures and all operating supply voltages. See the CXA3246Q/CXA3256R data sheets for a detailed description.)

- For the CMOS LOGIC at the rear end of the A/D converters
  DSYNC signal from CXA3266Q vs. A/D converter clock output
  The set-up time is T–3.0ns and the hold time is T–1.0ns.



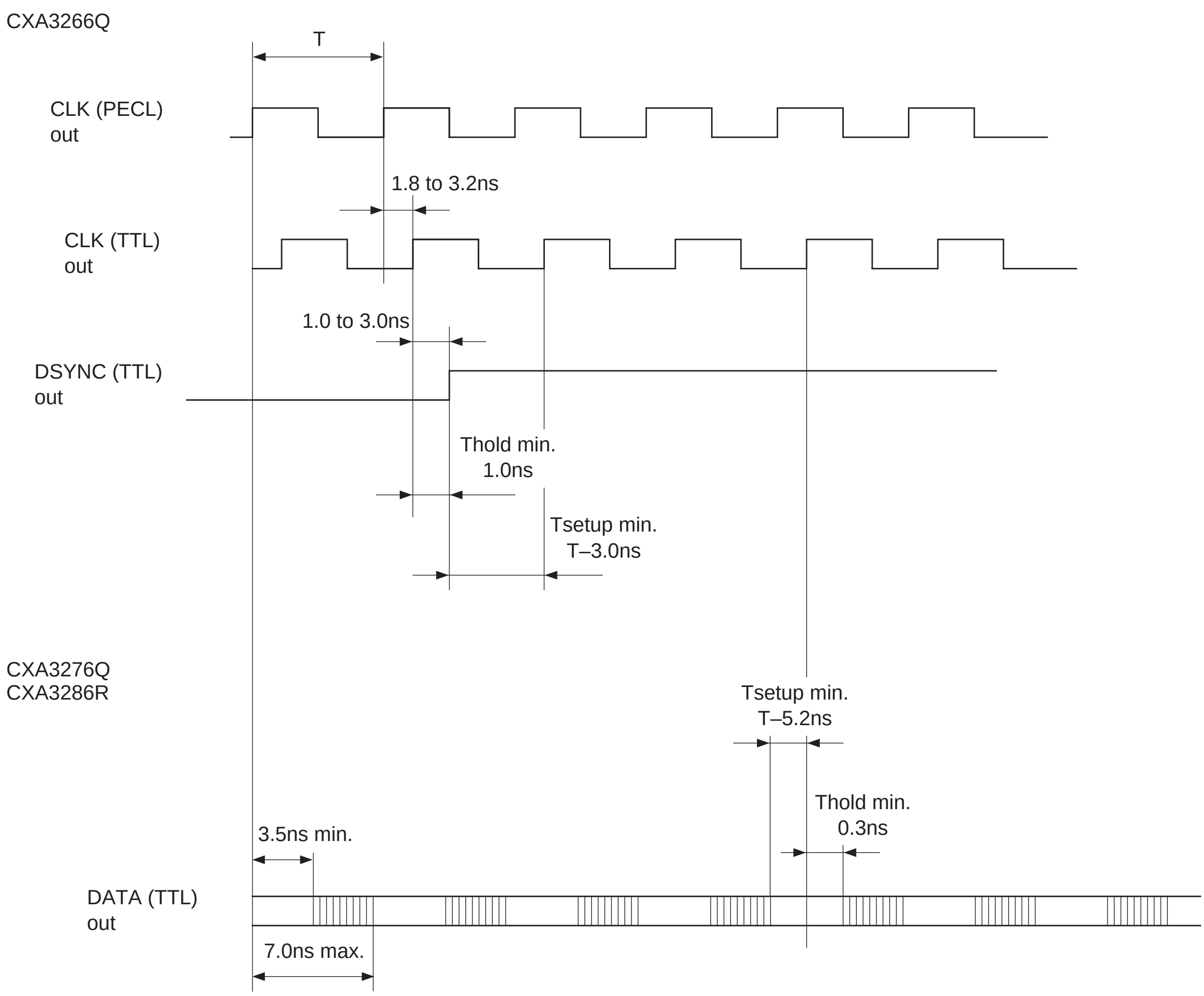
CXA3266Q and Sony ADC (Straight Mode) Timing: 100MHz specification

The CXA3266Q and CXA3276Q/CXA3286R timings are shown below.

Here, the important timings are as follows.
(The clock cycle is labeled as T.)

- For the CMOS LOGIC at the rear end of the A/D converters
  A/D converter data output vs. clock output from CXA3266Q
  The set-up time is T–5.2ns and the hold time is 0.3ns. (These timings also include combinations of three A/D converters from different lots, and are defined for all operating temperatures and all operating supply voltages. See the CXA3276Q/CXA3286R data sheets for a detailed description.)

- For the CMOS LOGIC at the rear end of the A/D converters
  DSYNC signal from CXA3266Q vs. A/D converter clock output
  The set-up time is T–3.0ns and the hold time is T–1.0ns.



CXA3266Q-PWB (CXA3266Q Evaluation Board)

The CXA3266Q-PWB is an evaluation board for the CXA3266Q PLL-IC. This board makes it possible to easily evaluate the CXA3266Q's performance using the supplied control program (Note: IBM PC/AT, MS-DOS 5.0 or newer US mode specifications).

Features

- Two input level (TTL and PECL) SYNC input
- Two output level (TTL and PECL) CLK, CLK2 and DSYNC output
- Supply voltage: +5.0V

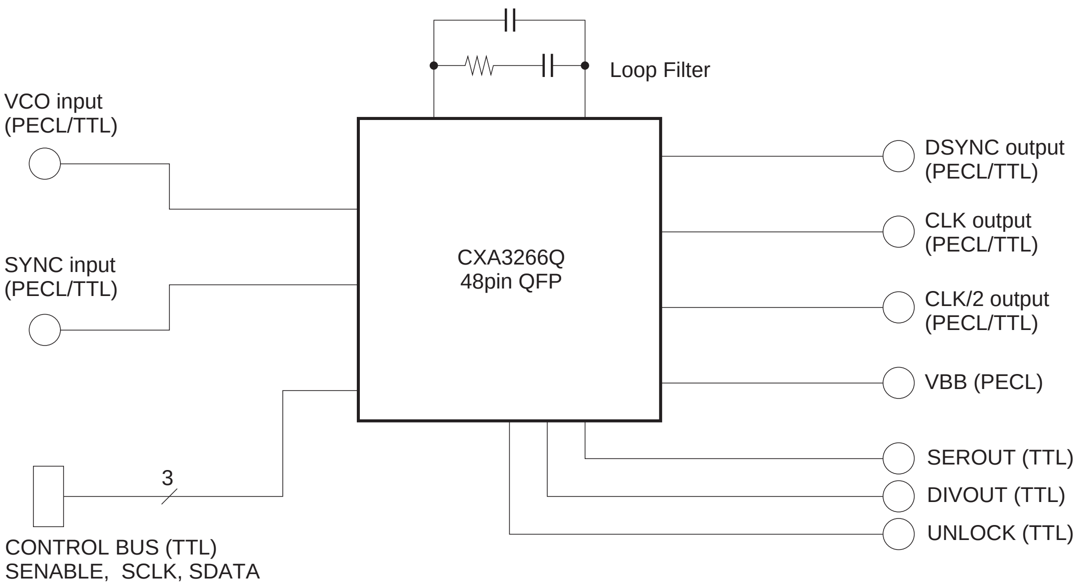
Absolute Maximum Ratings (Ta = 25°C)

Supply voltage	V_{CC}	–0.5 to +7.0	V

Recommended Operating Conditions

• Supply voltage	V_{CC}	4.75 to 5.25	V	
	GND	0	V	
• Digital input	(PECL)	DIN (High)	V_{CC} – 1.1	V (Min.)
		DIN (Low)	V_{CC} – 1.5	V (Max.)
	(TTL)	DIN (High)	GND + 2.0	V (Min.)
		DIN (Low)	GND + 0.8	V (Max.)
• Operating ambient temperature				
	Ta	–20 to +75	°C	

Block Diagram



Setting Methods and Notes on Operation

Input pins

This PWB supports TTL single and PECL complementary input.

Input pins:
- SYNC: TTL level input, 10 to 120kHz
- SYNCL: PECL low level input, 10 to 120kHz
- SYNCH: PECL high level input, 10 to 120kHz

- VCO: TTL level input. This is a test pin and is therefore normally not used.
- VCOL: PECL low level input. This is a test pin and is therefore normally not used.
- VCOH: PECL high level input. This is a test pin and is therefore normally not used.

Output pins

This PWB supports TTL single and PECL complementary output.

DSYNCH,
DSYNCL: PECL level complementary delay SYNC outputs. The output range is 10 to 120kHz.

DSYNC: TTL level delay SYNC output. The output range is 10 to 120kHz.

CLKH,
CLKL: PECL level complementary CLK outputs. The output range is 10 to 203MHz.

CLK,
CLKN: TTL level complementary CLK outputs. The output range is 10 to 100MHz.

CLK/2H,
CLK/2L: PECL level complementary 1/2 CLK outputs. The output range is 5 to 100MHz.

CLK/2,
CLK/2N: TTL level complementary CLK outputs. The output range is 5 to 100MHz.

VBB: Outputs the PECL amplitude threshold voltage.

SEROUT: TTL level control register serial data output.
DIVOUT: TTL level internal programmable counter test output.
UNLOCK: TTL level UNLOCK output. This pin requires external circuits such as appropriate capacitors and resistors.
See the IC specifications for a detailed description.

PECL outputs (VBB, DSYNCH, DSYNCL, CLKH, CLKL, CLK/2H, CLK/2L) are output constantly, but TTL outputs (DSYNC, CLK, CLKN, CLK/2, CLK/2N, SEROUT, DIVOUT, UNLOCK) are controlled by the respective control registers. Therefore, the enable/disable settings should be made in accordance with the application. See the following pages for the setting method.

Jumper Wire Settings

S1, S2: These enable/disable HOLD (Pin 6). HOLD is active high, so the jumper wire should be connected to S2 (HOLD = low) for normal use. When using HOLD, connect the jumper wire to S1 (HOLD = high). (For the initial setting, the jumper wire is connected to S2.)

S3, S4: These enable/disable TLOAD (Pin 13). Connect the jumper wire to S4 (TLOAD = high) for normal use. When using TLOAD, connect the jumper wire to S3 (TLOAD = low). (For the initial setting, the jumper wire is connected to S4.)

S5, S6: These enable/disable CS (Pin 14). Connect the jumper wire to S6 (CS = high) for normal use. When using Power Save, connect the jumper wire to S5 (CS = low). (For the initial setting, the jumper wire is connected to S6.)

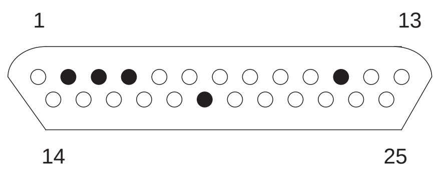
Supplied Program

This PWB has a control program that facilitates evaluation of the CXA3266Q. Operation methods and precautions are as follows.

1) Compatible personal computers
Use an IBM PC/AT or compatible machine equipped with a 25-pin D-SUB parallel port (printer port). Also, operating systems which support the program are MS-DOS 5.0 or newer and MS-Windows 3.1 or newer. (When using Windows, start the program from the DOS window.)

2) Connection of the supplied cable
Connect the supplied cable to the parallel port of the personal computer and the DBUS1 connector of the CXA3266Q-PWB.

D-SUB 25-pin parallel connector pin arrangement



Pin 2 : SCLK
Pin 3 : SDATA
Pin 4 : SENABLE
Pin 11 : SERIN
Pin 19 : GND

3) Connect the power cable and supply power to the CXA3266Q-PWB.

4) Start the program
A) Boot the personal computer and then shift to the directory containing the program.
B) Set MS-DOS to US mode. → US Return or Enter
C) Input the program name. → CXA3266Q Return or Enter → Move to the program screen.

5) Description of program screen

A) Setting of each function

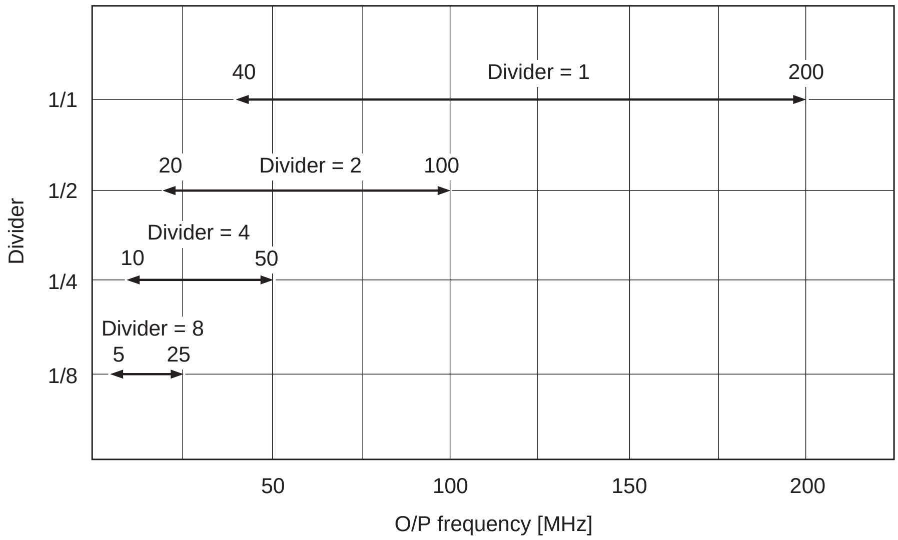
When the program is started, the following initial screen is displayed.

```
                              A3266 PLL REGISTERS

                                 Divisor 1672
                                 Divider 2

   Coarse Delay 00                                 Fine Delay  0
                                                   Charge Pump 00

      Polarity                     Power
   SYNC   DSYNC   PD             SCAN   SYNTH              VCO Bypass
    0      0      0               ON     ON                    ON

      O/P Enable
   DIVOUT      UNLOCK     DSYNC      CLK2      NCLK2      CLK1      NCLK1
     ON          ON         ON        ON         ON         ON        ON

      DSYNC Functions
   DELAY       WIDTH      HOLD      BYPASS
    ON           00        ON         ON

Use arrow keys to select data bit. Press ENTER to toggle and load data.
Use Pg Up and Pg Dn to increment/decrement divisor and fine delay registers.
Press a to abort, s to scan registers          MIXED SIGNAL SYSTEMS AUG 1998
```

Divisor

This is used to input the frequency division ratio of the program counter. The value can be changed as desired from 9 to 4111 by moving the cursor to the position of the number and pressing the Return or Enter key. (Note: The operating range of the CXA3266Q is from 256 to 4096.) The value can also be incremented or decremented by one step by pressing the Page Up or Page Down key, respectively.

The internal VCO has an oscillator frequency of 40 to 200MHz, so the output frequency and Divider (VCO frequency divider) setting range are as follows.



Divider

This sets the VCO output frequency division ratio to 1/1, 1/2, 1/4 or 1/8. The frequency division ratio changes repeatedly in the order of 1/1 → 1/2 → 1/4 → 1/8 → 1/1 each time the cursor is moved to the position of the number and the Return or Enter key is pressed.

Coarse Delay

This is the DSYNC upper delay time setting. The value can be changed by moving the cursor to the position of the number and pressing the Return or Enter key. The delay time variable range settings are "00" (2 CLK), "01" (3 CLK), "10" (4 CLK) or "11" (5 CLK).

Fine Delay

This is the DSYNC lower delay time setting. The value can be changed by moving the cursor to the position of the number and pressing the Return or Enter key. The value can also be incremented or decremented by one step by pressing the Page Up or Page Down key, respectively. The delay time can be varied from 1/32 CLK to 64/32 CLK by setting "0" to "63", respectively.

Charge Pump

This is the charge pump circuit KI setting. The value can be changed by moving the cursor to the position of the number and pressing the Return or Enter key. KI can be set to "00" (approximately 100µA), "01" (approximately 200µA), "10" (approximately 400µA) or "11" (approximately 800µA).

Polarity

These are the SYNC, DSYNC and PD (Phase Detector) polarity inversion settings, and should be set as necessary such as when inverting the SYNC input and DSYNC output waveforms. The setting value "1" is positive polarity, and "0" is negative polarity. These should normally all be set to "1". (Fix PD to "1" other than during test mode.)

Power

SCAN: This is the control register read setting. When this is ON, the control register serial data is output from SEROUT (Pin 15). This should normally be set to OFF.

SYNTH: This is the enable/disable setting for this IC. This should normally be set to ON.

VCO By-pass: This is set to OFF when testing the program counter. This should normally be set to ON.

O/P Enable

These are the enable/disable settings for each TTL output (DIVOUT, UNLOCK, DSYNC, CLK2, NCLK2, CLK1 and NCLK1). Set to ON when performing evaluation using TTL output.

DSYNC Functions

DELAY: When DIVOUT is output from DSYNC output, its delay is set. 4 CLK for OFF; 5 CLK for ON.

WIDTH: When DIVOUT is output from DSYNC output, its pulse width is changed. Their settings are 1 CLK for "00", 2 CLK for "01", 4 CLK for "10", and 8 CLK for "11".

HOLD: DSYNC output status is set during HOLD. Output OFF status for OFF (H or L fixed according to DSYNC POL polarity); DSYNC or DIVOUT are output for ON.

BYPASS: DSYNC/DIVOUT output switching from DSYNC output is performed. DSYNC is output for ON; DIVOUT for OFF.

B) Description of readout mode

This program has a function (readout mode) that reads the contents written to the control registers from the CXA3266Q SEROUT (Pin 15) and displays these contents on the screen. This function is described below.

1) Set SCAN to ON at the function setting screen.
2) Press the S key.
   The following screen appears.

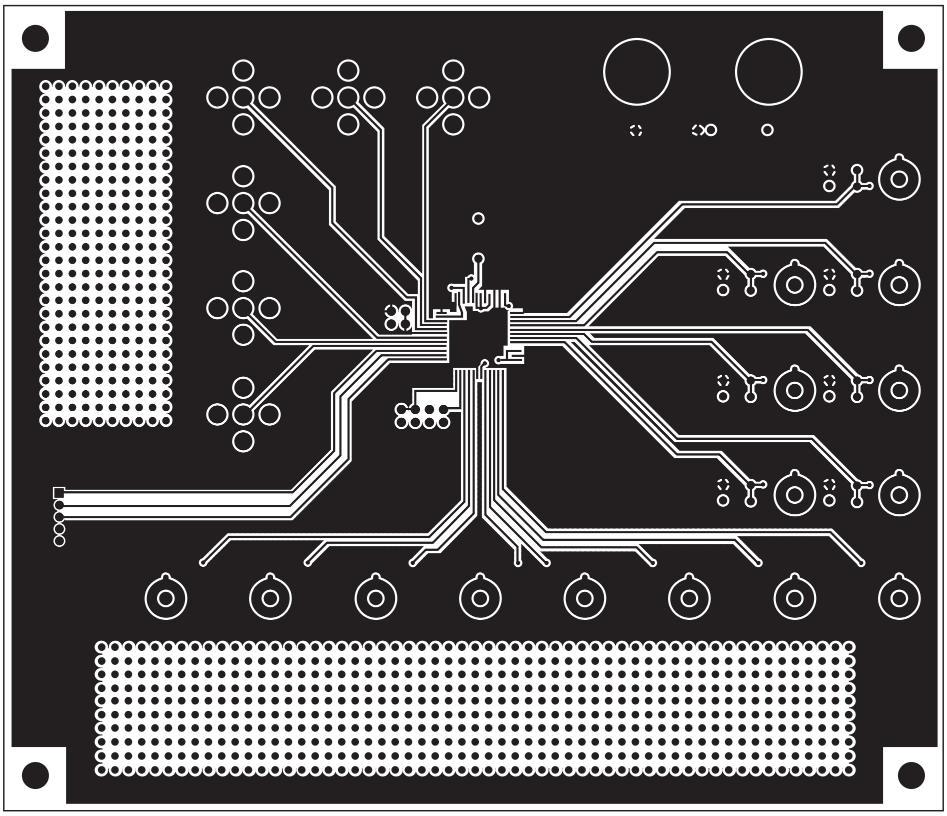
```
                    SCAN RESULT, CXA3266 PLL REGISTERS

       Register 1 DIVREG1     00111000
       Register 2 DIVREG2         0101
       Register 3 CENFREREG         01
       Register 4 DELAYREG    00100000
       Register 5 CPREG         100110
       Register 6 TTLPOLREG   11111111
       Register 7 TESTPOWREG    111111



Press r to return to PLL REGISTERS MENU.
Press a to abort                                MIXED SIGNAL SYSTEMS AUG 1998
```

This screen conforms to the Control Register Table listed in the CXA3266Q data sheet.

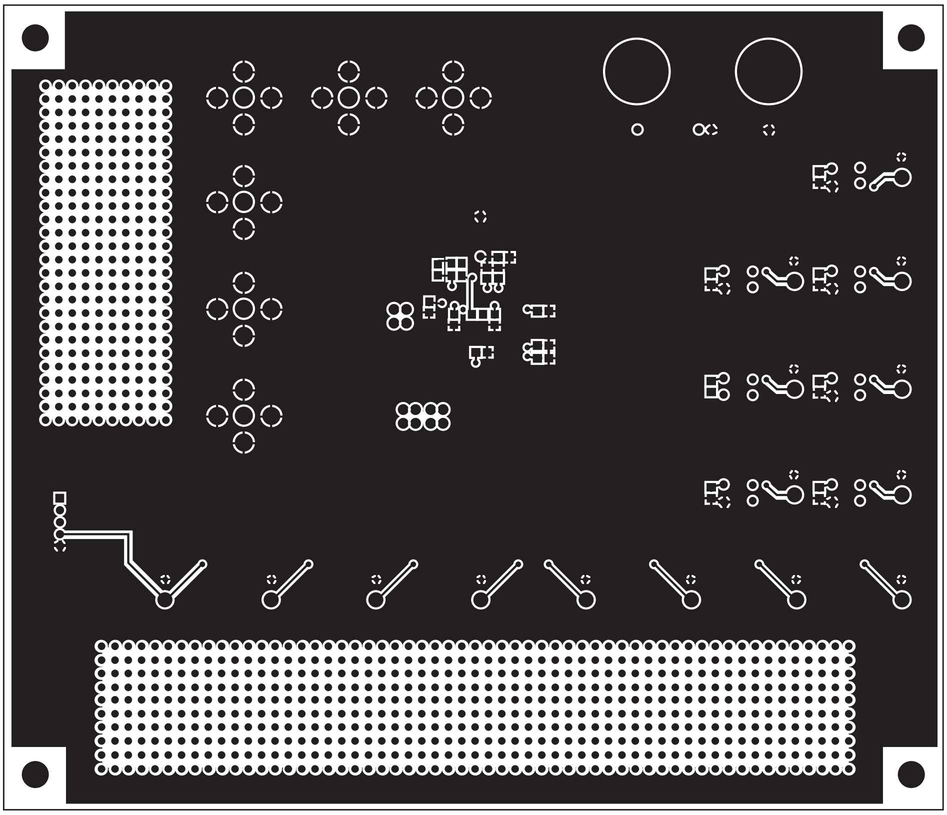
3) Press the R key to return to the original function setting screen.

C) Quit the program

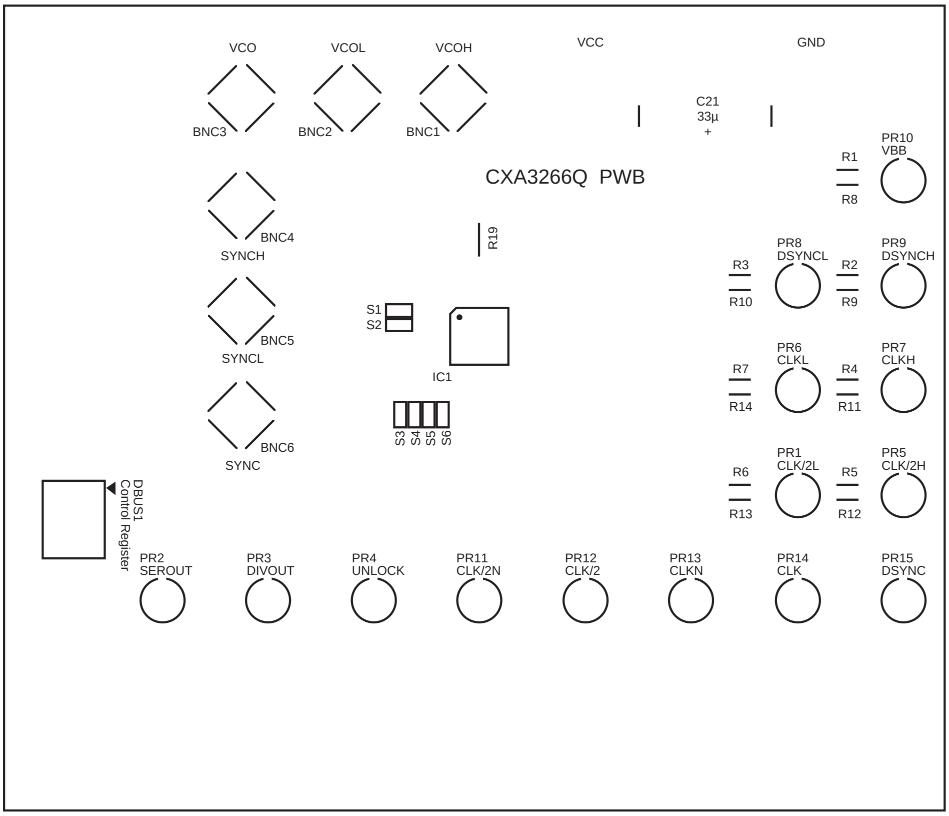
Press the A key to quit the program.



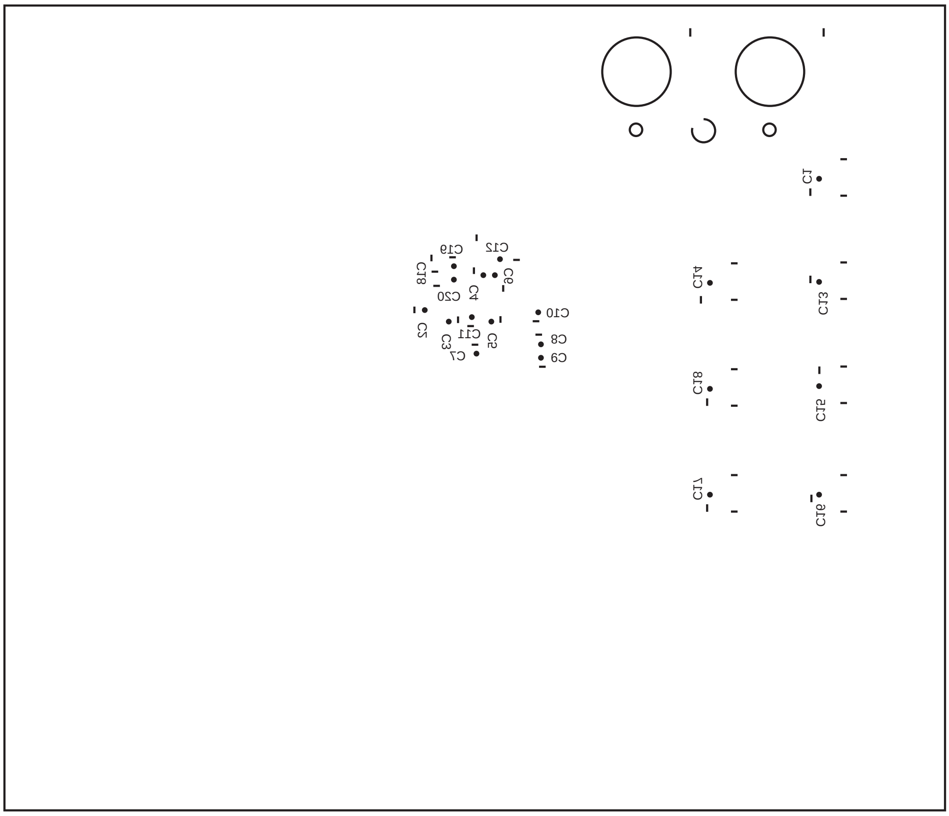
Substrate Pattern (parts surface)



Substrate Pattern (solder surface)

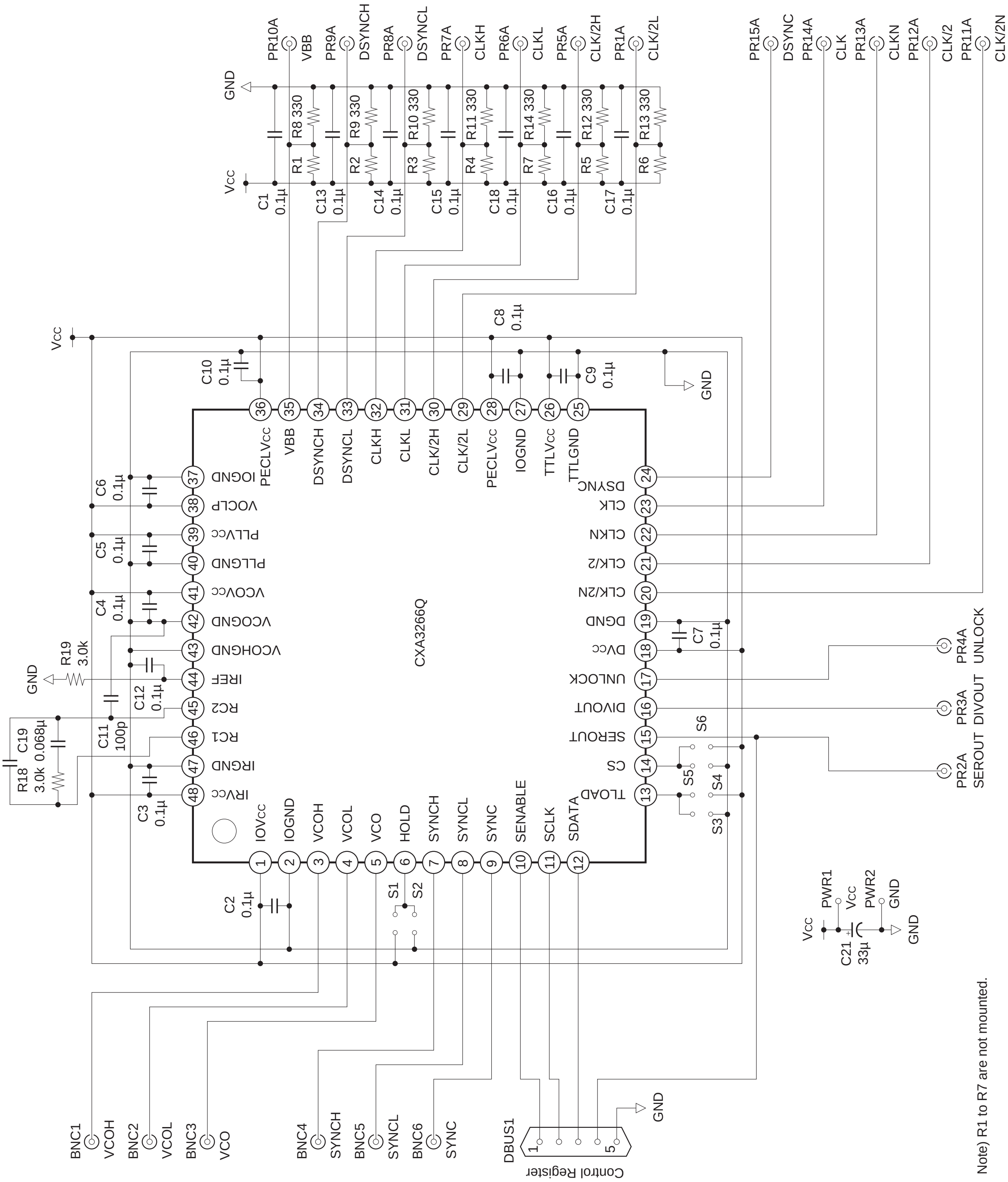


Silk Screen (parts surface)



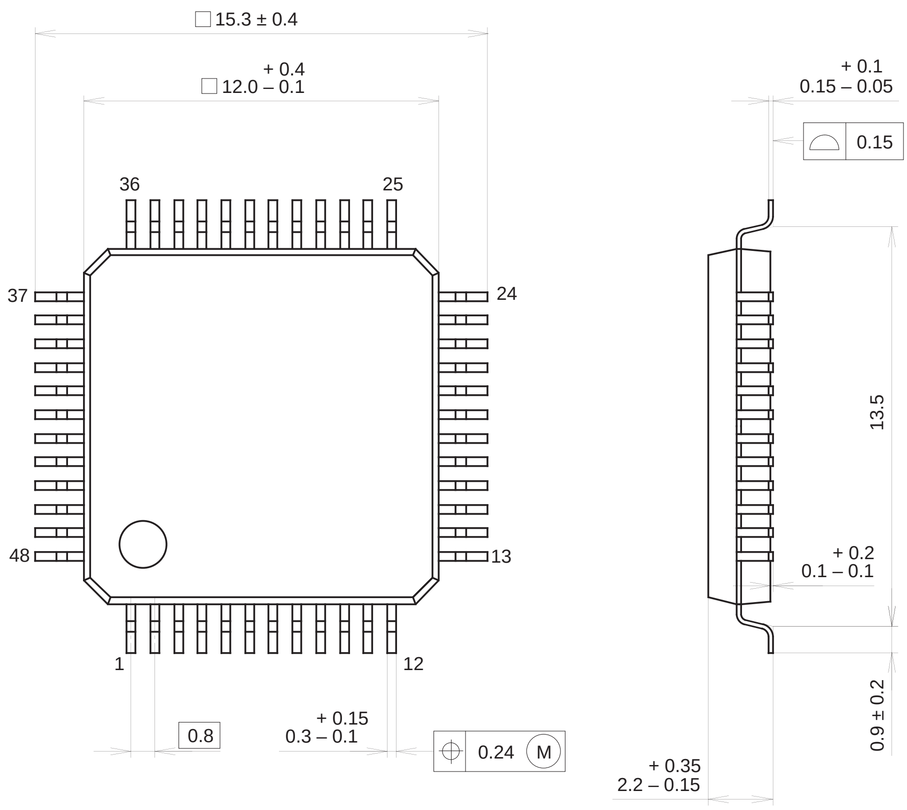
Silk Screen (solder surface)

PWB Circuit Diagram



Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).